YOVI 2008 Core

I2C Bus Interface

(IIC)

Function Specifications

Rev 0.00

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0.00	New created			Duong Dang 08/06/30

Index and Table

1. Scope

This document is the Function Specification of I2C Bus Interface.

2. Features

I^2C Bus Interface has the following features:

- Selection of addressing format or non-addressing format
- Conforms to Phillips I^2C bus interface
- Two ways of setting slave address
- Start and stop conditions generated automatically in master mode
- Selection of acknowledge output levels when receiving
- Automatic loading of acknowledge bit when transmitting
- Wait function in master mode
- Wait function
- Interrupt sources
- Selection of 32 internal clocks
- Direct bus drive

3. Block Diagram

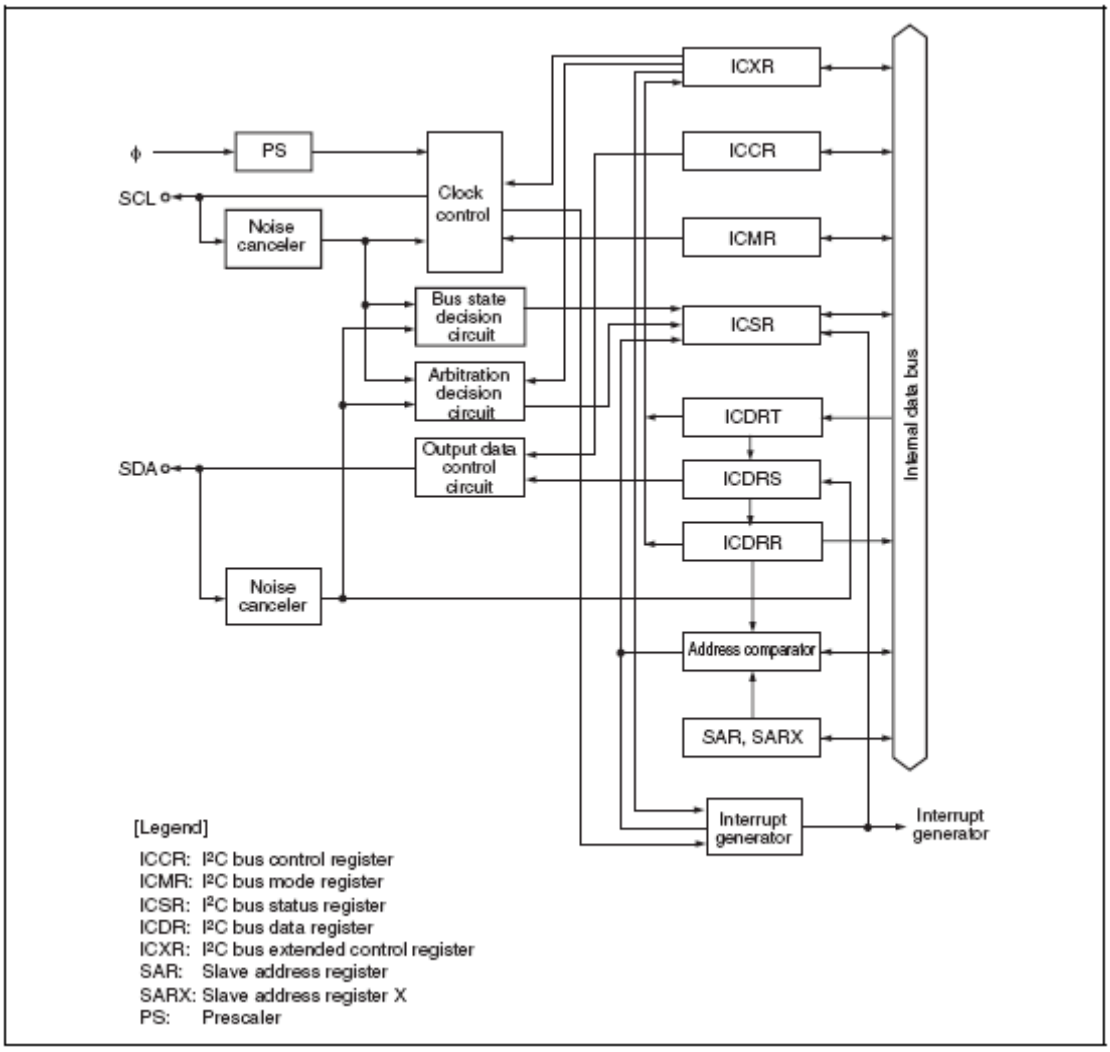

Figure 3.1: IIC block diagram

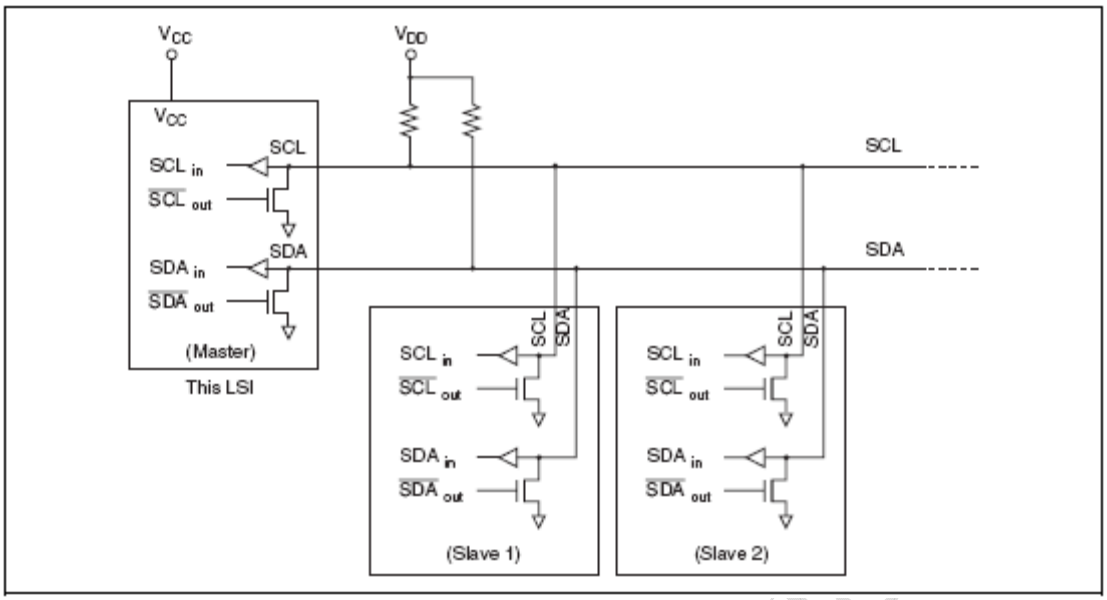

Figure 3.2: I²C Bus Interface Connections (Example: This LSI as Master)

4. Port Descriptions

Table below shows the IIC port description

Name	I/O	Function
SCL0	Input/Output	Clock input/output pin of channel IIC_0
SDA0	Input/Output	Clock input/output pin of channel IIC_0
SCL1	Input/Output	Clock input/output pin of channel IIC_1
SDA1	Input/Output	Clock input/output pin of channel IIC_1
SCL2	Input/Output	Clock input/output pin of channel IIC_2
SDA2	Input/Output	Clock input/output pin of channel IIC_2
SCL3	Input/Output	Clock input/output pin of channel IIC_3
SDA3	Input/Output	Clock input/output pin of channel IIC_3
SCL4	Input/Output	Clock input/output pin of channel IIC_4
SDA4	Input/Output	Clock input/output pin of channel IIC_4
SCL5	Input/Output	Clock input/output pin of channel IIC_5
SDA5	Input/Output	Clock input/output pin of channel IIC_5

Table 4.1: Port Description

5. Register Descriptions

This IIC has the following registers:

- I^2C bus data register (ICDR)
- Slave address register (SAR)
- Second slave address register (SARX)
- I^2C bus mode register (ICMR)
- I^2C bus transfer rate select register (IICX3)
- I^2C bus control register (ICCR)
- I^2C bus status register (ICSR)
- I^2C bus extended control register (ICXR)
- I^2C SMbus control register (ICSMBCR)

5.1 I2C bus data register (ICDR)

ICDR:

- An 8 bit readable/writable register.
- Such as a transmit data register and a receive data register.
- Be divided internally into a shift register (ICDRS), receive buffer (ICDRR) and transmit buffer (ICDRT).
- Writing transmit data to ICDR:
  - In master transmit mode:
    - Writing transmit data to ICDR should be performed after start condition detection.
    - When the start condition is detected, previous write data is ignored.

  - In slave transmit mode:
    - Writing should be performed after the slave addresses match.
    - TRS bit is automatically changed to 1.
  - Data transferred automatically from ICDRT to ICDRS:
    - If IIC is in transmit mode (TRS = 1) and the next data is in ICDRT (the ICDRE flag is 0).
    - If The ICDRE flag is 1 and the next transmit data writing is waited.
  - No data is transferred from ICDRT to ICDRS:
    - IIC is in receive mode (TRS = 0).

- Reading receive data from ICDR:
  - Is performed after data is transferred from ICDRS to ICDRR.
  - Data is transferred from ICDRS to ICDRR:
    - If IIC is in receive mode and no previous data remains in ICDRR (the ICDRF flag is 0).
    - If additional data is received while the ICDRF flag is 1.
  - No data is transferred from ICDRS to ICDRR:
    - Is in transmit mode

- Transmit data should be written justified toward the MSB side when MLS = 0 in ICMR and toward the LSB side when MLS = 1.
- Receive data bits should be read from the LSB side when MLS = 0 and from the MSB side when MLS = 1.
- ICDR can be written to and read from only when the ICE bit is set to 1 in ICCR.
- The initial value of ICDR is undefined.

Bit	7	6	5	4	3	2	1	0
Initial value								
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

5.2 Slave Address Register (SAR)

SAR:

- Sets the slave address and selects the communication format.
- LSI operates as the slave device
  - LSI in slave mode.
  - If the FS bit is set to 0 and the upper 7 bits of SAR match the upper 7 bits of the first frame received after a start condition.
- Can be accessed only when the ICE bit in ICCR is cleared to 0.

Bit	7	6	5	4	3	2	1	0
	SVAX6	SVAX5	SVAX4	SVAX3	SVAX2	SVAX1	SVAX0	FSX
Initial value	0	0	0	0	0	0	0	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	SVAX6	All 0	R/W	Second Slave Address
6	SVAX5			Set the second slave address.
5	SVAX4			
4	SVAX3			
3	SVAX2			
2	SVAX1			
1	SVAX0			
0	FSX	1	R/W	Format Select X Selects the communication format together with the FS bit in SAR. Refer to table 15.2.

SAR FS	SARX FSX	Operating Mode
0	0	I²C bus format • SAR and SARX slave addresses recognized • General call address recognized
	1	I²C bus format • SAR slave address recognized • SARX slave address ignored • General call address recognized
1	0	I²C bus format • SAR slave address ignored • SARX slave address recognized • General call address ignored
	1	Clocked synchronous serial format • SAR and SARX slave addresses ignored • General call address ignored

Figure 5.1: Transfer format

5.3 I2C Bus Mode Register (ICMR)

ICMR:

- Sets the communication format and transfer rate.
- Can only be accessed when the ICE bit in ICCR is set to 1.

Bit	7	6	5	4	3	2	1	0
	MLS	WAIT	CKS2	CKS1	CKS0	BC2	BC1	BC0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	MLS	0	R/W	MSB-First/LSB-First Select 0: MSB-first 1: LSB-first Set this bit to 0 when the I²C bus format is used.
6	WAIT	0	R/W	Wait Insertion Bit This bit is valid only in master mode with the I²C bus format. 0: Data and the acknowledge bit are transferred consecutively with no wait inserted. 1: After the fall of the clock for the final data bit (8th clock), the IRIC flag is set to 1 in ICCR, and a wait state begins (with SCL at the low level). When the IRIC flag is cleared to 0 in ICCR, the wait ends and the acknowledge bit is transferred. For details, refer to section 15.4.7, IRC Setting Timing and SCL Control.
5 4 3	CKS2 CKS1 CKS0	All 0	R/W	Transfer Clock Select These bits are used only in master mode. These bits select the required transfer rate, together with the IICX5 (channel 5), IICX4 (channel 4), and IICX3 (channel 3) bits in IICX3, and the IICX2 (channel 2), IICX1 (channel 1), and IICX0 (channel 0) bits in STCR. Refer to table 15.3.
2 1 0	BC2 BC1 BC0	All 0	R/W	Bit Counter These bits specify the number of bits to be transferred next. Bit BC2 to BC0 settings should be made during an interval between transfer frames. If bits BC2 to BC0 are set to a value other than B'000, the setting should be made while the SCL line is low. The bit counter is initialized to B'000 when a start condition is detected. The value returns to B'000 at the end of a data transfer. I²C Bus Format — Clocked Synchronous Serial Mode B'000: 9 bits — B'000: 8 bits B'001: 2 bits — B'001: 1 bits B'010: 3 bits — B'010: 2 bits B'011: 4 bits — B'011: 3 bits B'100: 5 bits — B'100: 4 bits B'101: 6 bits — B'101: 5 bits B'110: 7 bits — B'110: 6 bits B'111: 8 bits — B'111: 7 bits

5.4 I2C Bus Transfer Rate Select Register (IICX3)

IICX3:

Selects the IIC transfer rate clock and sets the transfer rate of IIC channels 3 to 5.

Bit	7	6	5	4	3	2	1	0
					TCSS	IICX5	IICX4	IICX3
Initial value					0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	—	—	Reserved These bits cannot be modified.
3	TCSS	0	R/W	Transfer Rate Clock Source Select This bit selects a clock rate to be applied to the I²C bus transfer rate. 0: ϕ/2 1: ϕ/4
2 1 0	IICX5 IICX4 IICX3	All 0	R/W	IIC Transfer Rate Select These bits are used to control IIC operation. These bits select the transfer rate in master mode, together with the CKS2 to CKS0 bits in ICMR. For the transfer rate, see table 15.3. IICX5, IICX4, and IICX3 control IIC_5, IIC_4, and IIC_3, respectively

- TCSS = 0

STCR/ IICX3	ICMR Bit 5	ICMR Bit 4	ICMR Bit 3		Transfer Rate (MHz)						
IICXn	CKS2	CKS1	CKS0	Clock	φ = 5 MHz	φ = 8 MHz	φ = 10 MHz	φ = 16 MHz	φ = 20 MHz	φ = 25 MHz	φ = 33 MHz
0	0	0	0	φ/28	178.6	285.7	357.1	571.4*1	714.3*1	892.9*1	1178.6*1
			1	φ/40	125.0	200.0	250.0	400.0	500.0*1	625.0*1	825.0*1
		1	0	φ/48	104.2	166.7	208.3	333.3	416.7*1	520.8*1	697.5*1
			1	φ/64	78.1	125.0	156.3	250.0	312.5	390.6	515.6*1
	1	0	0	φ/80	62.5	100.0	125.0	200.0	250.0	312.5	412.5*1
			1	φ/100	50.0	80.0	100.0	160.0	200.0	250.0	330.0*2
		1	0	φ/112	44.6	71.4	89.3	142.9	178.6	223.2	294.6*2
			1	φ/128	39.1	62.5	78.1	125.0	156.3	195.3	257.8*2
1	0	0	0	φ/56	89.3	142.9	178.6	285.7	357.1	446.4*1	589.3*1
			1	φ/80	62.5	100.0	125.0	200.0	250.0	312.5	412.5*1
		1	0	φ/96	52.1	83.3	104.2	166.7	208.3	260.4	343.8
			1	φ/128	39.1	62.5	78.1	125.0	156.3	195.3	257.8
	1	0	0	φ/160	31.3	50.0	62.5	100.0	125.0	156.3	206.3
			1	φ/200	25.0	40.0	50.0	80.0	100.0	125.0	165.0
		1	0	φ/224	22.3	35.7	44.6	71.4	89.3	111.6	147.3
			1	φ/256	19.5	31.3	39.1	62.5	78.1	97.7	128.9

Notes: 1. The correct operation cannot be guaranteed since the value is outside the I²C bus interface specifications (high-speed mode: max. 400 kHz)
2. When operate IIC in this setting, see 5 in section 15.6, Usage Notes.
(n = 0 to 5)

Figure 5.2: I²C bus Transfer Rate (1)

- TCSS = 1

STCR/ IICX3	ICMR Bit 5	ICMR Bit 4	ICMR Bit 3		Transfer Rate (MHz)						
IICXn	CKS2	CKS1	CKS0	Clock	φ = 5 MHz	φ = 8 MHz	φ = 10 MHz	φ = 16 MHz	φ = 20 MHz	φ = 25 MHz	φ = 33 MHz
0	0	0	0	φ/56	89.3	142.9	178.6	285.7	357.1	446.4*	589.3*
			1	φ/80	62.5	100.0	125.0	200.0	250.0	312.5	412.5*
		1	0	φ/96	52.1	83.3	104.2	166.7	208.3	260.4	343.8
			1	φ/128	39.1	62.5	78.1	125.0	156.3	195.3	257.8
	1	0	0	φ/160	31.3	50.0	62.5	100.0	125.0	156.3	206.3
			1	φ/200	25.0	40.0	50.0	80.0	100.0	125.0	165.0
		1	0	φ/224	22.3	35.7	44.6	71.4	89.3	111.6	147.3
			1	φ/256	19.5	31.3	39.1	62.5	78.1	97.7	128.9
1	0	0	0	φ/112	44.6	71.4	89.3	142.9	178.6	223.2	294.6
			1	φ/160	31.3	50.0	62.5	100.0	125.0	156.3	206.3
		1	0	φ/190	26.0	41.7	52.1	83.3	104.2	130.2	171.9
			1	φ/256	19.5	31.3	39.1	62.5	78.1	97.7	128.9
	1	0	0	φ/320	15.6	25.0	31.3	50.0	62.5	78.1	103.1
			1	φ/400	12.5	20.0	25.0	40.0	50.0	62.5	82.5
		1	0	φ/448	11.2	17.9	22.3	35.7	44.6	55.8	73.7
			1	φ/512	9.8	15.6	19.5	31.3	39.1	48.8	64.5

Note: * The correct operation cannot be guaranteed since the value is outside the I²C bus interface specifications (high-speed mode: max. 400 kHz)
(n = 0 to 5)

Figure 5.3: I²C bus Transfer Rate (2)

5.5 I2C Bus Control Register (ICCR)

ICCR:

- Controls the I²C bus interface and performs interrupt flag confirmation.

Bit	7	6	5	4	3	2	1	0
	ICE	ICIE	MST	TRS	ACKE	BBSY	IRIC	SCP
Initial value					0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W*[3]	R/W*[1]	R/W*[1]

Bit	Bit Name	Initial Value	R/W	Description
7	ICE	0	R/W	I^2C Bus Interface Enable 0: I^2C bus interface modules are stopped and I^2C bus interface module internal state is initialized. SAR and SARX can be accessed. 1: I^2C bus interface modules can perform transfer and reception, they are connected to the SCL and SDA pins, and the I^2C bus can be driven. ICMR and ICDR can be accessed.
6	IEIC	0	R/W	I^2C Bus Interface Interrupt Enable 0: Disables interrupts from the I^2C bus interface to the CPU 1: Enables interrupts from the I^2C bus interface to the CPU.
5	MST	0	R/W	Master/Slave Select
4	TRS	0	R/W	Transmit/Receive Select 00: Slave receive mode 01: Slave transmit mode 10: Master receive mode 11: Master transmit mode Both these bits will be cleared by hardware when they lose in a bus contention in master mode of the I^2C bus format. In slave receive mode with I^2C bus format, the R/$\overline{W}$ bit in the first frame immediately after the start condition automatically sets these bits in receive mode or transmit mode by hardware. Modification of the TRS bit during transfer is deferred until transfer is completed, and the changeover is made after completion of the transfer.

5 4	MST TRS	0 0	R/W R/W	[MST clearing conditions] (1) When 0 is written by software (2) When lost in bus contention in I^2C bus format master mode [MST setting conditions] (1) When 1 is written by software (for MST clearing condition 1) (2) When 1 is written in MST after reading MST = 0 (for MST clearing condition 2) [TRS clearing conditions] (1) When 0 is written by software (except for TRS setting condition 3) (2) When 0 is written in TRS after reading TRS = 1 (for TRS setting condition 3) (3) When lost in bus contention in I^2C bus format master mode [TRS setting conditions] (1) When 1 is written by software (except for TRS clearing condition 3) (2) When 1 is written in TRS after reading TRS = 0 (for TRS clearing condition 3) (3) When 1 is received as the R/$\overline{W}$ bit after the first frame address matching in I^2C bus format slave mode
3	ACKE	0	R/W	Acknowledge Bit Decision Selection 0: The value of the acknowledge bit is ignored, and continuous transfer is performed. The value of the received acknowledge bit is not indicated by the ACKB bit in ICSR, which is always 0. 1: If the acknowledge bit is 1, continuous transfer is halted. Depending on the receiving device, the acknowledge bit may be significant, in indicating completion of processing of the received data, for instance, or may be fixed at 1 and have no significance.

2	BBSY	0	R/W*[3]	Bus Busy
0	SCP	1	W	Start Condition/Stop Condition Prohibit In master mode • Writing 0 in BBSY and 0 in SCP: A stop condition is issued • Writing 1 in BBSY and 0 in SCP: A start condition and a restart condition are issued In slave mode • Writing to the BBSY flag is disabled. [BBSY setting condition] • When the SDA level changes from high to low under the condition of SCL = high, assuming that the start condition has been issued. [BBSY clearing conditions] • When the SDA level changes from low to high under the condition of SCL = high, assuming that the stop condition has been issued. To issue a start/stop condition, use the MOV instruction. The I^2C bus interface must be set in master transmit mode before the issue of a start condition. Set MST to 1 and TRS to 1 before writing 1 in BBSY and 0 in SCP. The BBSY flag can be read to check whether the I^2C bus (SCL, SDA) is busy or free.

1	IRIC	0	R/(W)*1	I²C Bus Interface Interrupt Request Flag Indicates that the I²C bus interface has issued an interrupt request to the CPU. IRIC is set at different times depending on the FS bit in SAR and the WAIT bit in ICMR. See section 15.4.7, IRIC Setting Timing and SCL Control. The conditions under which IRIC is set also differ depending on the setting of the ACKE bit in ICCR. [Setting conditions] I²C bus format master mode: • When a start condition is detected in the bus line state after a start condition is issued (when the ICDRE flag is set to 1 because of first frame transmission) • When a wait is inserted between the data and acknowledge bit when the WAIT bit is 1 (fall of the 8th transmit/receive clock) • At the end of data transfer (rise of the 9th transmit/receive clock) • When a slave address is received after bus mastership is lost • If 1 is received as the acknowledge bit (when the ACKB bit in ICSR is set to 1) when the ACKE bit is 1 • When the AL flag is set to 1 after bus mastership is lost while the ALIE bit is 1 I²C bus format slave mode: • When the slave address (SVA or SVAX) matches (when the AAS or AASX flag in ICSR is set to 1) and at the end of data transfer up to the subsequent retransmission start condition or stop condition detection (rise of the 9th clock) • When the general call address is detected (when the 0 is received for R/$\overline{W}$ bit, and ADZ flag in ICSR is set to 1) and at the end of data reception up to the subsequent retransmission start condition or stop condition detection (rise of the 9th receive clock) • When 1 is received as an acknowledge bit while the ACKE bit is 1 (when the ACKB bit is set to 1) • When a stop condition is detected while the STOPIM bit is 0 (when the STOP or ESTP flag in ICSR is set to 1)

1	IRIC	0	R/(W)*1	At the end of data transfer in clock synchronous serial format (rise of the 8th transmit/receive clock) When a start condition is detected with serial format selected When a condition occurs in which the ICDRE or ICDRF flag is set to 1. • When a start condition is detected in transmit mode (when a start condition is detected and the ICDRE flag is set to 1) • When transmitting the data in the ICDR register buffer (when data is transferred from ICDRT to ICDRS in transmit mode and the ICDRE flag is set to 1, or data is transferred from ICDRS to ICDRR in receive mode and the ICDRF flag is set to 1.) [Clearing conditions] • When 0 is written in IRIC after reading IRIC = 1 • When ICDR is accessed by DTC *2 (This may not be a clearing condition. For details, see the description of the DTC operation on the next page.

Notes: 1. Only 0 can be written to clear the flag to 0.
2. The DTC does not support IIC_4 and IIC_5.
3. If the BBSY bit is written to, the value of the flag is not changed.

When DTC is used:

- IRIC is cleared automatically.
- IRIR transfer can be performed continuously without CPU intervention.
- DTC does not support IIC_4 and IIC_5.

When with the I^2C bus format selected:

- IRIC is set to 1.
- An interrupt is generated.
- Other flags must be checked in order to identify the source that set IRIC to 1.

When ICDRE or ICDRF flag is set:

- IRTR flag may or may not be set.

- IRTR flag (the DTC start request flag) is not set at the end of a data transfer up to detection of a retransmission start condition or stop condition after a slave address (SVA).
- Or general call address match in I^2C bus format slave mode.

When the IRIC flag and IRTR flag are set:

- The ICDRE and ICDRF flag may not be set.
- The IRIC and IRTR flag are not cleared at the end of the specified number of transfer in continuous transfer using the DTC.
- The ICDRE or ICDRF flag is cleared, however, since the specified number of ICDR reads or writes have been completed.

MST	TRS	BBSY	ESTP	STOP	IRTR	AASX	AL	AAS	ADZ	ACKB	ICDRF	ICDRE	State
1	1	0	0	0	0	0↓	0	0↓	0↓	0	—	0	Idle state (flag clearing required)
1	1	1↑	0	0	1↑	0	0	0	0	0	—	1↑	Start condition detected
1	—	1	0	0	—	0	0	0	0	—	—	—	Wait state
1	1	1	0	0	—	0	0	0	0	1↑	—	—	Transmission end (ACKE=1 and ACKB=1)
1	1	1	0	0	1↑	0	0	0	0	0	—	1↑	Transmission end with ICDRE=0
1	1	1	0	0	—	0	0	0	0	0	—	0↓	ICDR write with the above state
1	1	1	0	0	—	0	0	0	0	0	—	1	Transmission end with ICDRE=1
1	1	1	0	0	—	0	0	0	0	0	—	0↓	ICDR write with the above state or after start condition detected
1	1	1	0	0	1↑	0	0	0	0	0	—	1↑	Automatic data transfer from ICDRT to ICDRS with the above state
1	0	1	0	0	1↑	0	0	0	0	—	1↑	—	Reception end with ICDRF=0
1	0	1	0	0	—	0	0	0	0	—	0↓	—	ICDR read with the above state
1	0	1	0	0	—	0	0	0	0	—	1	—	Reception end with ICDRF=1
1	0	1	0	0	—	0	0	0	0	—	0↓	—	ICDR read with the above state
1	0	1	0	0	1↑	0	0	0	0	—	1↑	—	Automatic data transfer from ICDRS to ICDRR with the above state
0↓	0↓	1	0	0	—	0	1↑	0	0	—	—	—	Arbitration lost
1	—	0↓	0	0	—	0	0	0	0	—	—	0↓	Stop condition detected

[Legend]

0: 0-state retained 1: 1-state retained —: Previous state retained

0↓: Cleared to 0 1↑: Set to 1

Figure 5.4: Flags and Transfer States (Master Mode)

MST	TRS	BBSY	ESTP	STOP	IRTR	AASX	AL	AAS	ADZ	ACKB	ICDRF	ICDRE	State
0	0	0	0	0	0	0	0	0	0	0	—	0	Idle state (flag clearing required)
0	0	1↑	0	0	0	0↓	0	0	0	0	—	1↑	Start condition detected
0	1↑/0 *1	1	0	0	0	0	—	1↑	0	0	1↑	1	SAR match in first frame (SARX≠SAR)
0	0	1	0	0	0	0	—	1↑	1↑	0	1↑	1	General call address match in first frame (SARX≠H'00)
0	1↑/0 *1	1	0	0	1↑	1↑	—	0	0	0	1↑	1	SAR match in first frame (SAR≠SARX)
0	1	1	0	0	—	—	—	—	0	1↑	—	—	Transmission end (ACKE=1 and ACKB=1)
0	1	1	0	0	1↑/0 *1	—	—	—	0	0	—	1↑	Transmission end with ICDRE=0
0	1	1	0	0	—	—	0↓	0↓	0	0	—	0↓	ICDR write with the above state
0	1	1	0	0	—	—	—	—	0	0	—	1	Transmission end with ICDRE=1
0	1	1	0	0	—	—	0↓	0↓	0	0	—	0↓	ICDR write with the above state
0	1	1	0	0	1↑/0 *2	—	0	0	0	0	—	1↑	Automatic data transfer from ICDRT to ICDRS with the above state
0	0	1	0	0	1↑/0 *2	—	—	—	—	—	1↑	—	Reception end with ICDRF=0
0	0	1	0	0	—	—	0↓	0↓	0↓	—	0↓	—	ICDR read with the above state

0	0	1	0	0	—	—	—	—	—	—	1	—	Reception end with ICDRF=1
0	0	1	0	0	—	—	0↓	0↓	0↓	—	0↓	—	ICDR read with the above state
0	0	1	0	0	1↑/0 *2	—	0	0	0	—	1↑	—	Automatic data transfer from ICDRS to ICDRR with the above state
0	—	0↓	1↑/0 *2	0/1↑ *3	—	—	—	—	—	—	—	0↓	Stop condition detected

[Legend]

0: 0-state retained 1: 1-state retained —: Previous state retained

0↓: Cleared to 0 1↑: Set to 1

Notes: 1. Set to 1 when 1 is received as a R/$\overline{W}$ bit following an address.

2. Set to 1 when the AASX bit is set to 1.

3. When ESTP=1, STOP is 0, or when STOP=1, ESTP is 0.

Figure 5.5: Flags and Transfer States (Slave Mode)

5.6 I2C Bus Status Register (ICSR)

ICSR consists of status flags.

Bit	7	6	5	4	3	2	1	0
	ESTP	STOP	IRTR	AASX	AL	AAS	ADZ	ACKB
Initial value	0	0	0	0	0	0	0	0
Read/Write	(R/W)*	(R/W)*	(R/W)*	(R/W)*	(R/W)*	(R/W)*	(R/W)*	(R/W)*

Bit	Bit Name	Initial Value	R/W	Description
7	ESTP	0	R/(W)*	Error Stop Condition Detection Flag This bit is valid in I²C bus format slave mode. [Setting condition] When a stop condition is detected during frame transfer. [Clearing conditions] • When 0 is written in ESTP after reading ESTP = 1 • When the IRIC flag in ICCR is cleared to 0
6	STOP	0	R/(W)*	Normal Stop Condition Detection Flag This bit is valid in I²C bus format slave mode. [Setting condition] When a stop condition is detected after frame transfer is completed. [Clearing conditions] • When 0 is written in STOP after reading STOP = 1 • When the IRIC flag is cleared to 0
5	IRTR	0	R/(W)*	I²C Bus Interface Continuous Transfer Interrupt Request Flag Indicates that the I²C bus interface has issued an interrupt request to the CPU, and the source is completion of reception/transmission of one frame in continuous transmission/reception for which DTC activation is possible. When the IRTR flag is set to 1, the IRIC flag is also set to 1 at the same time. [Setting conditions] I²C bus format slave mode: • When the ICDRE or ICDRF flag in ICDR is set to 1 when AASX = 1 I²C bus format master mode or clocked synchronous serial format mode: • When the ICDRE or ICDRF flag is set to 1 [Clearing conditions] • When 0 is written after reading IRTR = 1 • When the IRIC flag is cleared to 0 while ICE is 1

4	AASX	0	R/(W)*	Second Slave Address Recognition Flag In I²C bus format slave receive mode, this flag is set to 1 if the first frame following a start condition matches bits SVAX6 to SVAX0 in SARX. [Setting condition] When the second slave address is detected in slave receive mode and FSX = 0 in SARX [Clearing conditions] • When 0 is written in AASX after reading AASX = 1 • When a start condition is detected • In master mode
3	AL	0	R/(W)*	Arbitration Lost Flag Indicates that arbitration was lost in master mode. [Setting conditions] When ALSL=0 • If the internal SDA and SDA pin disagree at the rise of SCL in master transmit mode • If the internal SCL line is high at the fall of SCL in master mode When ALSL=1 • If the internal SDA and SDA pin disagree at the rise of SCL in master transmit mode • If the SDA pin is driven low by another device before the I²C bus interface drives the SDA pin low, after the start condition instruction was executed in master transmit mode [Clearing conditions] • When ICDR is written to (transmit mode) or read from (receive mode) • When 0 is written in AL after reading AL = 1

2	AAS	0	R/(W)*	Slave Address Recognition Flag In I²C bus format slave receive mode, this flag is set to 1 if the first frame following a start condition matches bits SVA6 to SVA0 in SAR, or if the general call address (H'00) is detected. [Setting condition] When the slave address or general call address (one frame including a R/$\overline{W}$ bit is H'00) is detected in slave receive mode and FS = 0 in SAR [Clearing conditions] • When ICDR is written to (transmit mode) or read from (receive mode) • When 0 is written in AAS after reading AAS = 1 • In master mode
1	ADZ	0	R/(W)*	General Call Address Recognition Flag In I²C bus format slave receive mode, this flag is set to 1 if the first frame following a start condition is the general call address (H'00). [Setting condition] When the general call address (one frame including a R/$\overline{W}$ bit is H'00) is detected in slave receive mode and FS = 0 or FSX = 0 [Clearing conditions] • When ICDR is written to (transmit mode) or read from (receive mode) • When 0 is written in ADZ after reading ADZ = 1 • In master mode If a general call address is detected while FS=1 and FSX=0, the ADZ flag is set to 1; however, the general call address is not recognized (AAS flag is not set to 1).

0	ACKB	0	R/W	Acknowledge Bit Stores acknowledge data. Transmit mode: [Setting condition] When 1 is received as the acknowledge bit when ACKE=1 in transmit mode [Clearing conditions] • When 0 is received as the acknowledge bit when ACKE=1 in transmit mode • When 0 is written to the ACKE bit Receive mode: 0: Returns 0 as acknowledge data after data reception 1: Returns 1 as acknowledge data after data reception When this bit is read, the value loaded from the bus line (returned by the receiving device) is read in transmission (when TRS = 1). In reception (when TRS = 0), the value set by internal software is read. When this bit is written, acknowledge data that is returned after receiving is rewritten regardless of the TRS value. If the ICSR register bit is written using bit-manipulation instructions, the acknowledge data should be re-set since the acknowledge data setting is rewritten by the ACKB bit reading value. Write the ACKE bit to 0 to clear the ACKB flag to 0, before transmission is ended and a stop condition is issued in master mode, or before transmission is ended and SDA is released to issue a stop condition by a master device.

Note: * Only 0 can be written to clear the flag.

5.7 I2C Bus Extended Control Register (ICXR)

ICXR:

- Enables or disables the I^2C bus interface interrupt generation and continuous receive operation.
- Indicates the status of receive/transmit operations.

Bit	7	6	5	4	3	2	1	0
	STOPIM	HNDS	ALIE	ICDRE	ALIE	ALSL	FNC1	FNC0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	STOPIM	0	R/W	Stop Condition Interrupt Source Mask Enables or disables the interrupt generation when the stop condition is detected in slave mode. 0: Enables IRIC flag setting and interrupt generation when the stop condition is detected (STOP = 1 or ESTP = 1) in slave mode. 1: Disables IRIC flag setting and interrupt generation when the stop condition is detected.
6	HNDS	0	R/W	Handshake Receive Operation Select Enables or disables continuous receive operation in receive mode. 0: Enables continuous receive operation 1: Disables continuous receive operation When the HNDS bit is cleared to 0, receive operation is performed continuously after data has been received successfully while ICDRF flag is 0. When the HNDS bit is set to 1, SCL is fixed to the low level after data has been received successfully while ICDRF flag is 0; thus disabling the next data to be transferred. The bus line is released and next receive operation is enabled by reading the receive data in ICDR.

5	ICDRF	0	R	Receive Data Read Request Flag Indicates the ICDR (ICDRR) status in receive mode. 0: Indicates that the data has been already read from ICDR (ICDRR) or ICDR is initialized. 1: Indicates that data has been received successfully and transferred from ICDRS to ICDRR, and the data is ready to be read out. [Setting conditions] • When data is received successfully and transferred from ICDRS to ICDRR. (1) When data is received successfully while ICDRF = 0 (at the rise of the 9th clock pulse). (2) When ICDR is read successfully in receive mode after data was received while ICDRF = 1. [Clearing conditions] • When ICDR (ICDRR) is read. • When 0 is written to the ICE bit. When ICDRF is set due to the condition (2) above, ICDRF is temporarily cleared to 0 when ICDR (ICDRR) is read; however, since data is transferred from ICDRS to ICDRR immediately, ICDRF is set to 1 again. Note that ICDR cannot be read successfully in transmit mode (TRS = 1) because data is not transferred from ICDRS to ICDRR. Be sure to read data from ICDR in receive mode (TRS = 0).

4	ICDRE	0	R	Transmit Data Write Request Flag Indicates the ICDR (ICDRT) status in transmit mode. 0: Indicates that the data has been already written to ICDR (ICDRT) or ICDR is initialized. 1: Indicates that data has been transferred from ICDRT to ICDRS and is being transmitted, or the start condition has been detected or transmission has been complete, thus allowing the next data to be written to. [Setting conditions] • When the start condition is detected from the bus line state in I^2C bus format or serial format. • When data is transferred from ICDRT to ICDRS. 1. When data is transmitted completely while ICDRE = 0 (at the rise of the 9th clock pulse). 2. When data is written to ICDR completely in transmit mode after data was transmitted while ICDRE = 1. [Clearing conditions] • When data is written to ICDR (ICDRT). • When the stop condition is detected in I^2C bus format or serial format. • When 0 is written to the ICE bit. Note that if the ACKE bit is set to 1 in I^2C bus format thus enabling acknowledge bit decision, ICDRE is not set when data is transmitted completely while the acknowledge bit is 1. When ICDRE is set due to the condition (2) above, ICDRE is temporarily cleared to 0 when data is written to ICDR (ICDRT); however, since data is transferred from ICDRT to ICDRS immediately, ICDRF is set to 1 again. Do not write data to ICDR when TRS = 0 because the ICDRE flag value is invalid during the time.

3	ALIE	0	R/W	Arbitration Lost Interrupt Enable Enables or disables IRIC flag setting and interrupt request when arbitration is lost. 0: Disables interrupt request when arbitration is lost. 1: Enables interrupt request when arbitration is lost.
2	ALSL	0	R/W	Arbitration Lost Condition Select Selects the condition under which arbitration is lost. 0: If the SDA pin state disagrees with the data that I²C bus interface outputs at the rise of SCL and the SCL pin is driven low by another device. 1: If the SDA pin state disagrees with the data that I²C bus interface outputs at the rise of SCL and the SDA line is driven low by another device in idle state or after the start condition instruction was executed.
1 0	FNC1 FNC0	0 0	R/W R/W	Function Bit These bits cancel some restrictions on usage. For details, refer to section 15.6, Usage Notes. 00: Restrictions on operation remaining in effect 01: Setting prohibited 10: Setting prohibited 11: Restrictions on operation canceled

5.8 I2C SMBus Control Register (ICSMBCR)

ICSMBCR:

- Used to support the System Management Bus (SMBus) specififcations.
- Support the SMBus specification.
- SDA output data hold time should be specified in the range of 300ns to 1000ns.
- When the SMBus is not supported, the initial value should not be change.
- ICSMBCR is enabled to access when bit MSTP4 is cleared to 0.

Bit	7	6	5	4	3	2	1	0
	SMB5E	SMB4E	SMB3E	SMB2E	SMB1E	SMB0E	FSEL1	FSEL0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 6 5 4 3 2	SMB5E SMB4E SMB3E SMB2E SMB1E SMB0E	All 0	R/W	SMBus Enable These bits enable/disable to support the SMBus, combining with bits FSEL1 and FSEL0. The SMB5E bit controls IIC_5, the SMB4E bit controls IIC_4, the SMB3E bit controls IIC_3, the SMB2E bit controls IIC_2, the SMB1E bit controls IIC_1, the SMB0E bit controls IIC_0. 0: Disables to support the SMBus 1: Enables to support the SMBus
1 0	FSEL1 FSEL0	0 0	R/W R/W	Frequency Selection These bits must be specified to match the system clock frequency in order to support the SMBus. For details of the setting, see table 15.7.

				Output Data Hold Time (ns)								
SMBnE	FSEL1	FSEL0	Min./ Max.	ϕ = 5 MHz	ϕ = 6.6 MHz	ϕ = 8 MHz	ϕ = 10 MHz	ϕ = 13.3 MHz	ϕ = 16 MHz	ϕ = 20 MHz	ϕ = 25 MHz	ϕ = 33 MHz
0	—	—	Min.	400	303	250*	200*	150*	125*	100*	80*	61*
			Max.	600	455	375	300	226*	188*	150*	120*	91*
1	0	0	Min.	600	455	375	300	226*	188*	150*	120*	91*
			Max.	1000*	758	625	500	376	313	250*	200*	152*
		1	Min.	800	606	500	400	301	250*	200*	160*	121*
			Max.	1400*	1061*	875	700	526	438	350	280*	212*
	1	0	Min.	1200*	909	750	600	451	375	300	240*	182*
			Max.	2200*	1667*	1375*	1100*	827	688	550	440	333
		1	Min.	2000*	1515*	1250*	1000*	752	625	500	400	303
			Max.	3800*	2879*	2375*	1900*	1429*	1188*	950	760	576

Notes: n = 0 to 5

* Since the value is outside the SMBus specification, it should not be set.

Figure 5.6: Output Data Hold Time

System Clock	SMBnE	FSEL1	FSEL0
5 to 6.6 MHz	0	0	0
6.6 to 10 MHz	1	0	0
10 to 13.3 MHz	1	0	1
13.3 to 20 MHz	1	1	0
20 to 33 MHz	1	1	1

n = 0 to 5

Figure 5.7: ISCMBCR Setting

6. Operations

6.1 I2C Bus Data Format

I^2C bus interface:

- Has an I^2C bus format and a serial format.
- Are addressing formats with an acknowledge bit.
- The first frame following a start condition always consists of 9 bits.

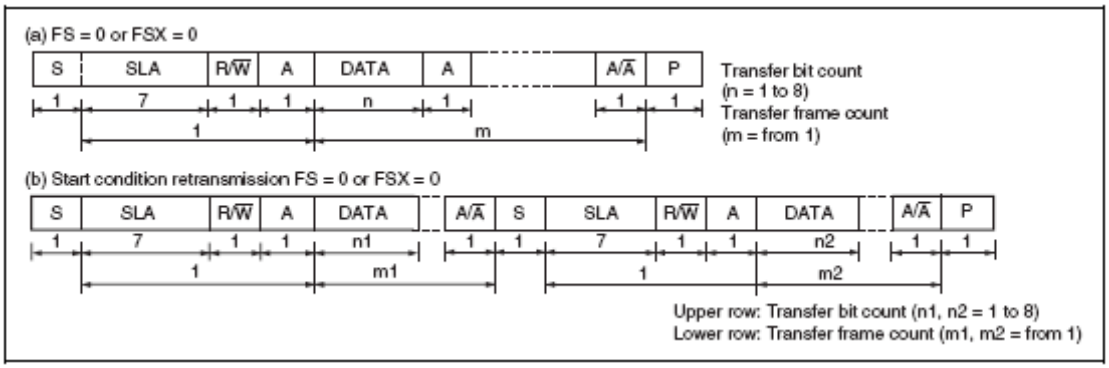

Figure 6.1: I^2C Bus Data Formats (I^2C Bus Formats)

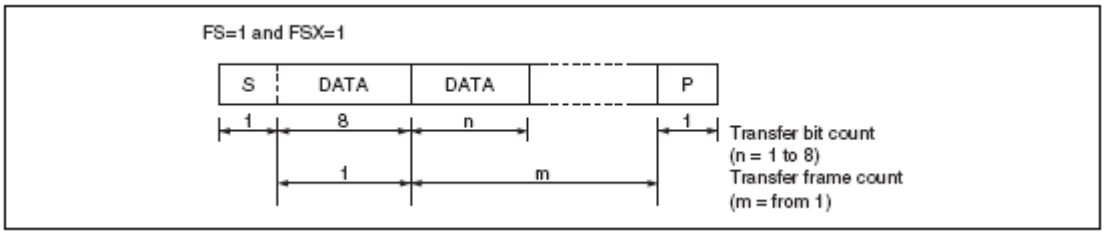

Figure 6.2: I^2C Bus Data Formats (Serial Formats)

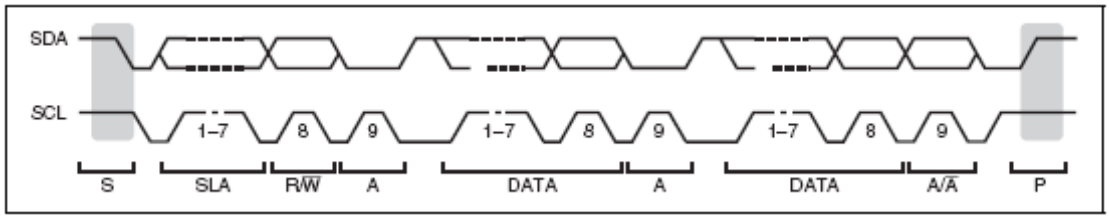

Figure 6.3: I^2C Bus Timing

Symbol	Description
S	Start condition. The master device drives SDA from high to low while SCL is high
SLA	Slave address. The master device selects the slave device.
R/$\overline{W}$	Indicates the direction of data transfer: from the slave device to the master device when R/$\overline{W}$ is 1, or from the master device to the slave device when R/W is 0
A	Acknowledge. The receiving device drives SDA low to acknowledge a transfer. (The slave device returns acknowledge in master transmit mode, and the master device returns acknowledge in master receive mode.)
DATA	Transferred data. The bit length of transferred data is set with the BC2 to BC0 bits in ICMR. The MSB first or LSB first is switched with the MLS bit in ICMR.
P	Stop condition. The master device drives SDA from low to high while SCL is high

Figure 6.4: I²C Bus Data Format Symbols

6.2 Initialization

Initialize the IIC by the procedure before starting transmission/reception of data.

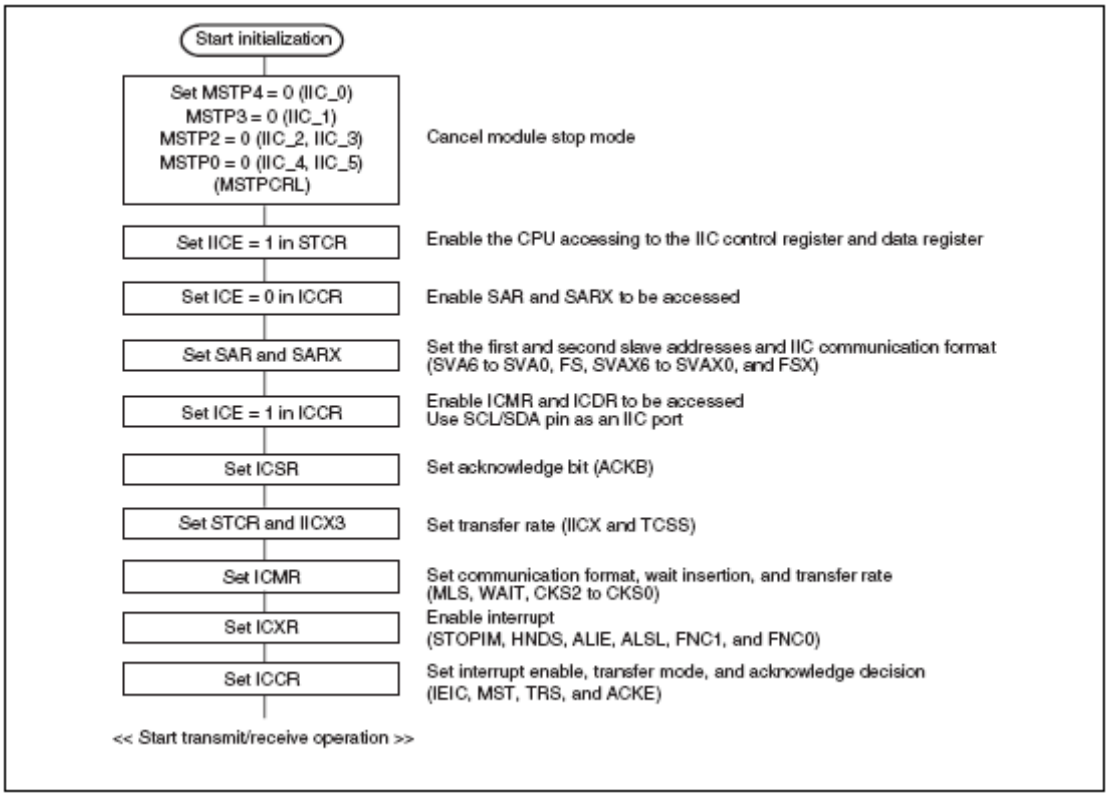

Figure 6.5: Sample flowchart for IIC Initialization

6.3 Master Transmit Operation

In I²C format master transmit mode, the master device outputs the transmit clock and transmit data, and the slave device returns an acknowledge signal.

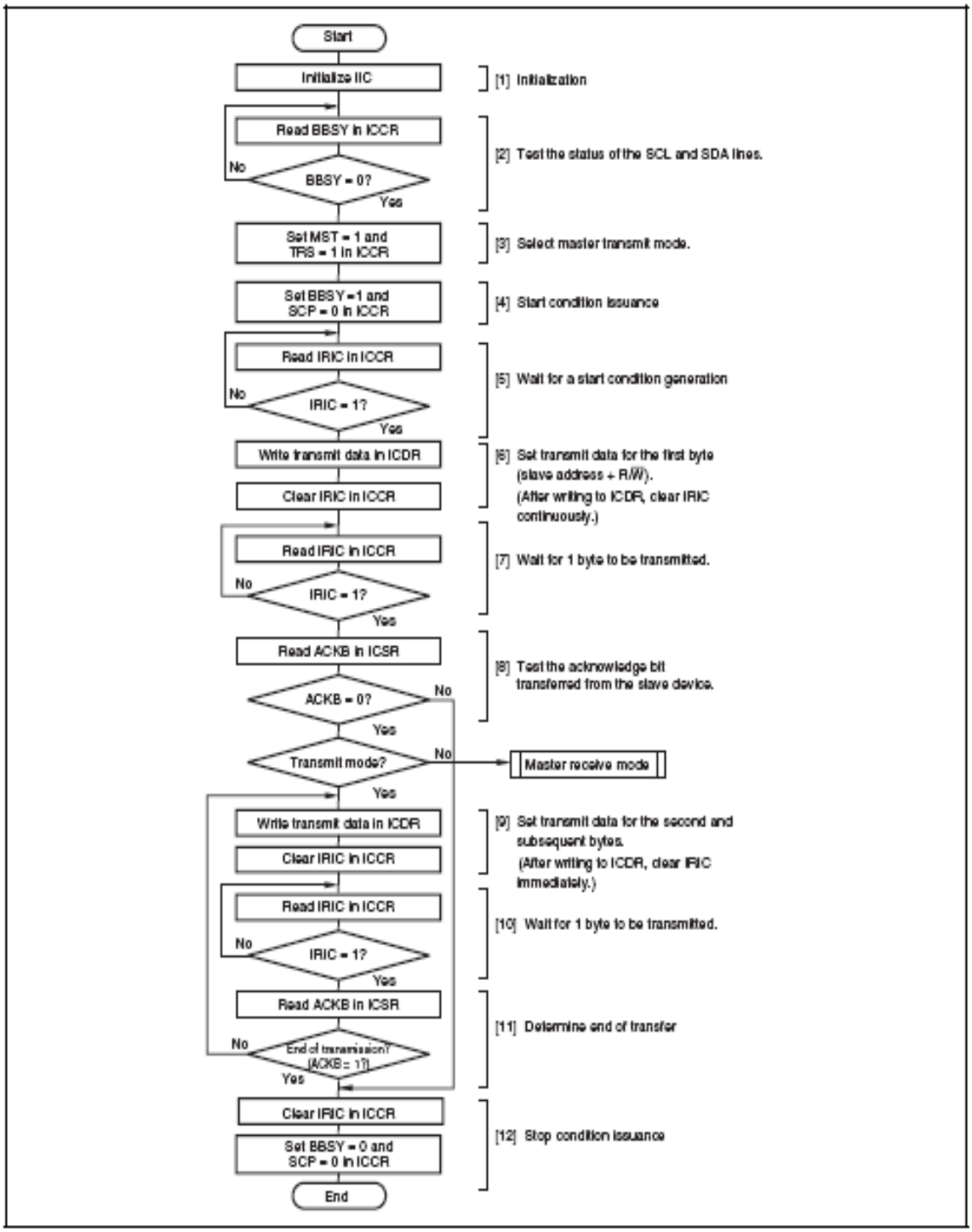

Figure 6.6: Sample Flowchart for Operations in Master Transmit Mode

The operation procedure and operations by which data is sequentially transmitted in synchronization with ICDR (ICDRT) write operations are:

[1] Initialize the IIC as described in section 15.4.2, Initialization.

[2] Read the BBSY flag in ICCR to confirm that the bus is free.

[3] Set bits MST and TRS to 1 in ICCR to select master transmit mode.

[4] Write 1 to BBSY and 0 to SCP in ICCR. This changes SDA from high to low when SCL is high, and generates the start condition.

[5] Then the IRIC and IRTR flags are set to 1. If the IEIC bit in ICCR has been set to 1, an interrupt request is sent to the CPU.

[6] Write the data (slave address + R/$\overline{W}$) to ICDR.

With the I^2C bus format (when the FS bit in SAR or the FSX bit in SARX is 0), the first frame data following the start condition indicates the 7-bit slave address and transmit/receive direction (R/$\overline{W}$).

To determine the end of the transfer, the IRIC flag is cleared to 0. After writing to ICDR, clear IRIC continuously so no other interrupt handling routine is executed. If the time for transmission of one frame of data has passed before the IRIC clearing, the end of transmission cannot be determined. The master device sequentially sends the transmission clock and the data written to ICDR. The selected slave device (i.e. the slave device with the matching slave address) drives SDA low at the 9th transmit clock pulse and returns an acknowledge signal.

[7] When one frame of data has been transmitted, the IRIC flag is set to 1 at the rise of the 9th transmit clock pulse. After one frame has been transmitted, SCL is automatically fixed low in synchronization with the internal clock until the next transmit data is written.

[8] Read the ACKB bit in ICSR to confirm that ACKB is cleared to 0. When the slave device has not acknowledged (ACKB bit is 1), operate step [12] to end transmission, and retry the transmit operation.

[9] Write the transmit data to ICDR.

[10] When one frame of data has been transmitted, the IRIC flag is set to 1 at the rise of the 9th transmit clock pulse. After one frame has been transmitted, SCL is automatically fixed low in synchronization with the internal clock until the next transmit data is written.

[11] Read the ACKB bit in ICSR.

Confirm that the slave device has been acknowledged (ACKB bit is 0). When there is still data to be transmitted, go to step [9] to continue the next transmission operation. When the slave device has not acknowledged (ACKB bit is set to 1), operate step [12] to end transmission.

[12] Clear the IRIC flag to 0.

Write 0 to ACKE in ICCR, to clear received ACKB contents to 0. Write 0 to BBSY and SCP in ICCR. This changes SDA from low to high when SCL is high, and generates the stop condition.

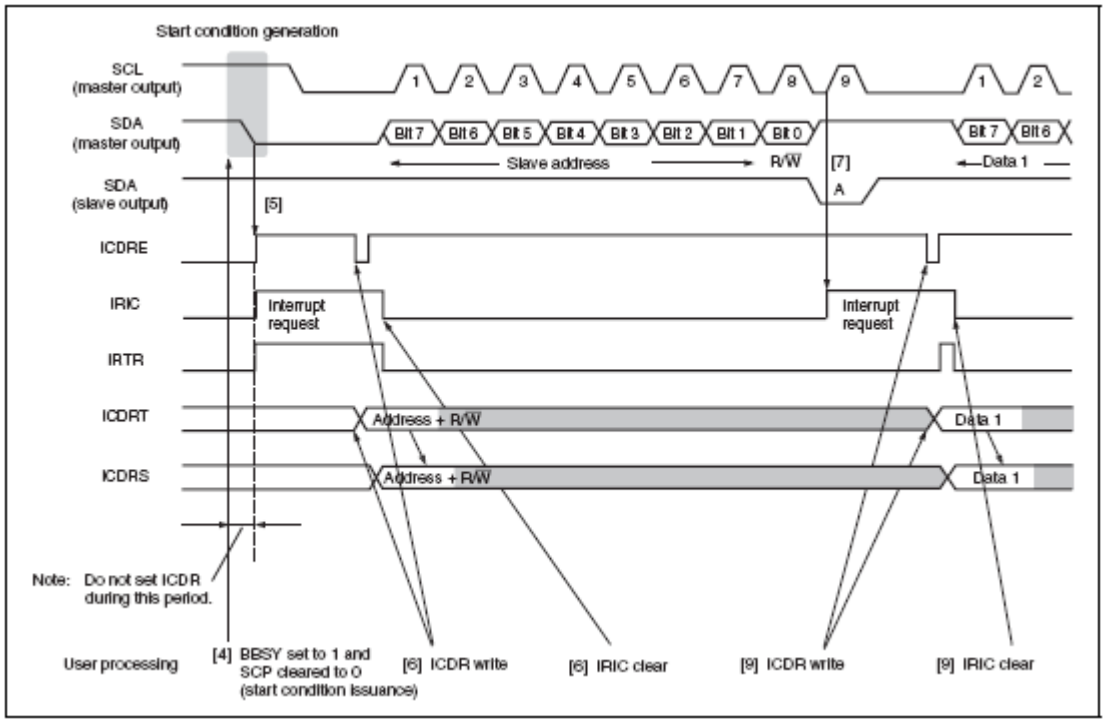

Figure 6.7: Operation Timing Example in Master Transmit Mode (MLS = WAIT = 0)

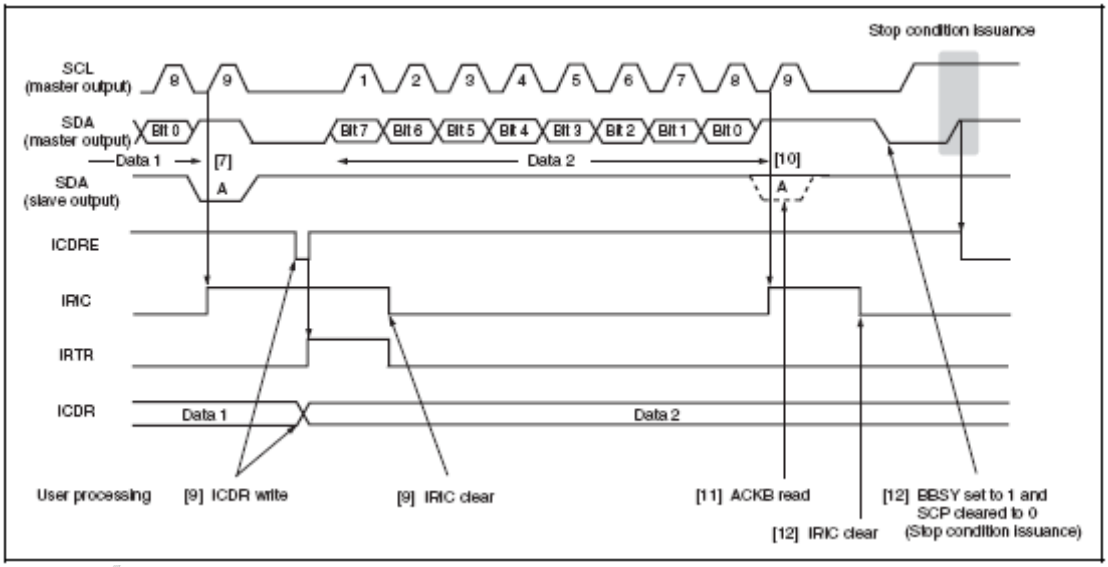

Figure 6.8: Stop Condition Issuance operation Timing Example in Master Transmit Mode (MLS = WAIT = 0)

6.4 Master Receive Operation

In I^2C bus format master receive mode:

- The master device outputs the receive clock
- Receive data
- Return an acknowledge signal.
- The slave device transmits data.

The master device transmits data containing the slave address and R/W (1:read) in the first frame following the start condition issuance in master transmit mode, selects the slave device, and then switches the mode for receive operation.

Receive Operation Using the HNDS Function (HNDS = 1)

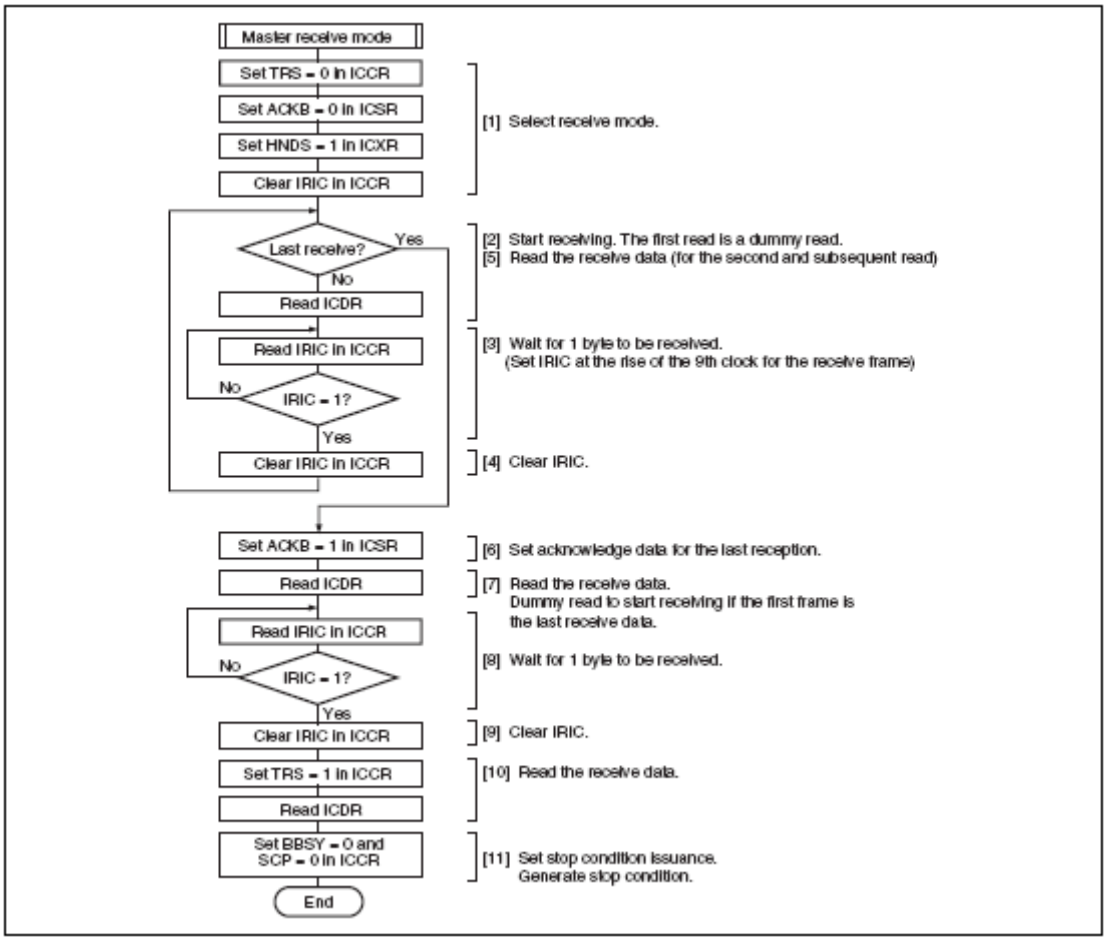

Figure 6.9: Sample Flowchart for Operations in Master Receive Mode (HNDS = 1)

The reception procedure and operations by which the data reception process is provided in 1-byte units with SCL fixed low at each data reception are described below:

[1] Clear the TRS bit in ICCR to 0 to switch from transmit mode to receive mode.
Clear the ACKB bit in ICSR to 0 (acknowledge data setting).
Set the HNDS bit in ICXR to 1.
Clear the IRIC flag to 0 to determine the end of reception.
Go to step [6] to halt reception operation if the first frame is the last receive data.

[2] When ICDR is read (dummy data read), reception is started, and the receive clock is output, and data received, in synchronization with the internal clock. (Data from the SDA pin is sequentially transferred to ICDRS in synchronization with the rise of the receive clock pulses.)

[3] The master device drives SDA low to return the acknowledge data at the 9th receive clock pulse. The receive data is transferred to ICDRR from ICDRS at the rise of the 9th clock pulse, setting the ICDRF, IRIC, and IRTR flags to 1. If the IEIC bit has been set to 1, an interrupt request is sent to the CPU.
The master device drives SCL low from the fall of the 9th receive clock pulse to the ICDR data reading.

[4] Clear the IRIC flag to determine the next interrupt.
Go to step [6] to halt reception operation if the next frame is the last receive data.

[5] Read ICDR receive data. This clears the ICDRF flag to 0. The master device outputs the receive clock continuously to receive the next data.
Data can be received continuously by repeating steps [3] to [5].

[6] Set the ACKB bit to 1 so as to return the acknowledge data for the last reception.

[7] Read ICDR receive data. This clears the ICDRF flag to 0. The master device outputs the receive clock to receive data.

[8] When one frame of data has been received, the ICDRF, IRIC, and IRTR flags are set to 1 at the rise of the 9th receive clock pulse.

[9] Clear the IRIC flag to 0.

[10] Read ICDR receive data after setting the TRS bit. This clears the ICDRF flag to 0.

[11] Clear the BBSY bit and SCP bit to 0 in ICCR. This changes SDA from low to high when SCL is high, and generates the stop condition.

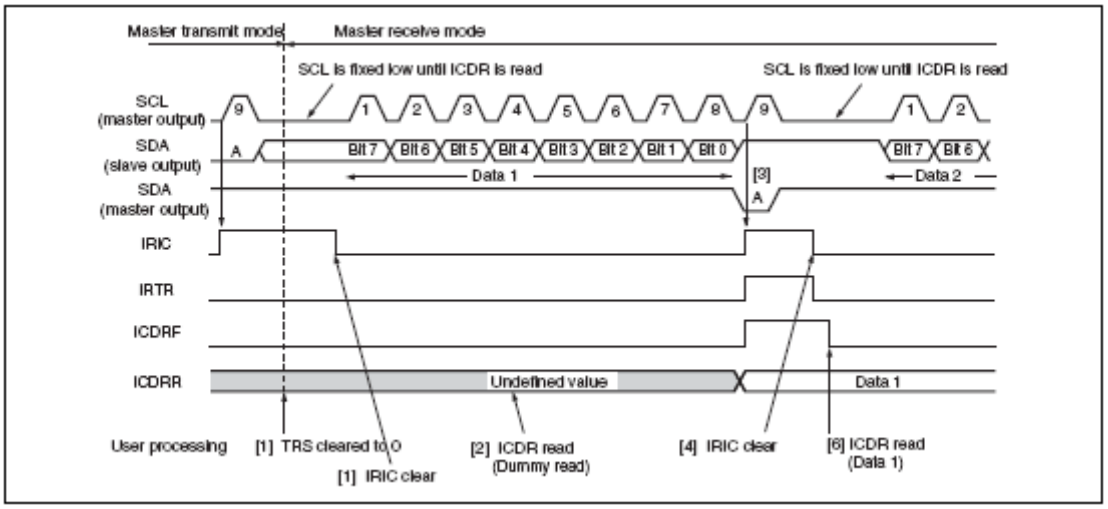

Figure 6.10: Master Receive Mode Operation Timing Example (MLS = WAIT = 0, HNDS = 1)

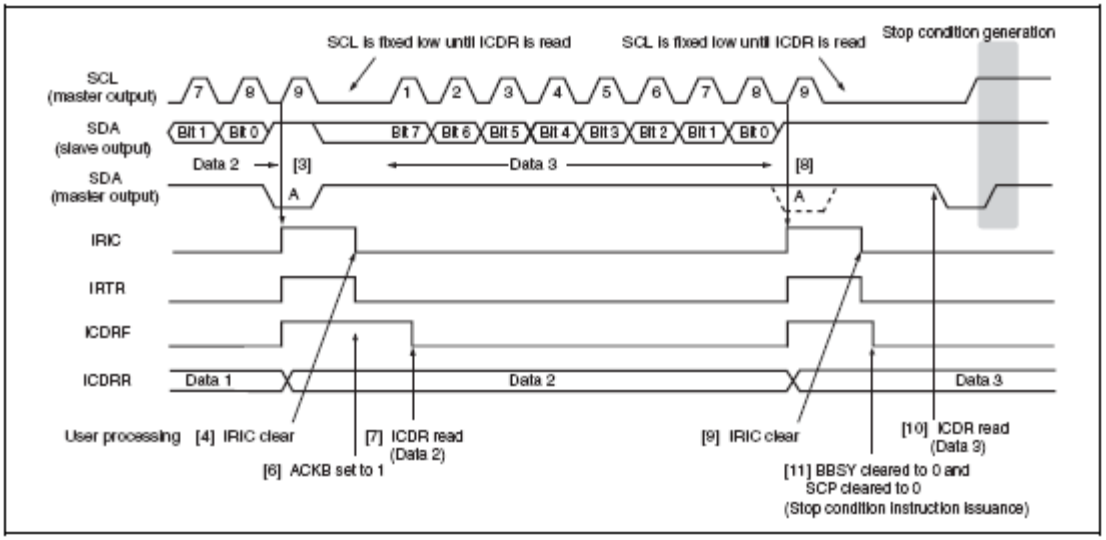

Figure 6.11: Stop Condition Issuance Timing Example in Master Receive Mode (MLS = WAIT = 0, HNDS = 1)

Receive Operation Using the Wait Function:

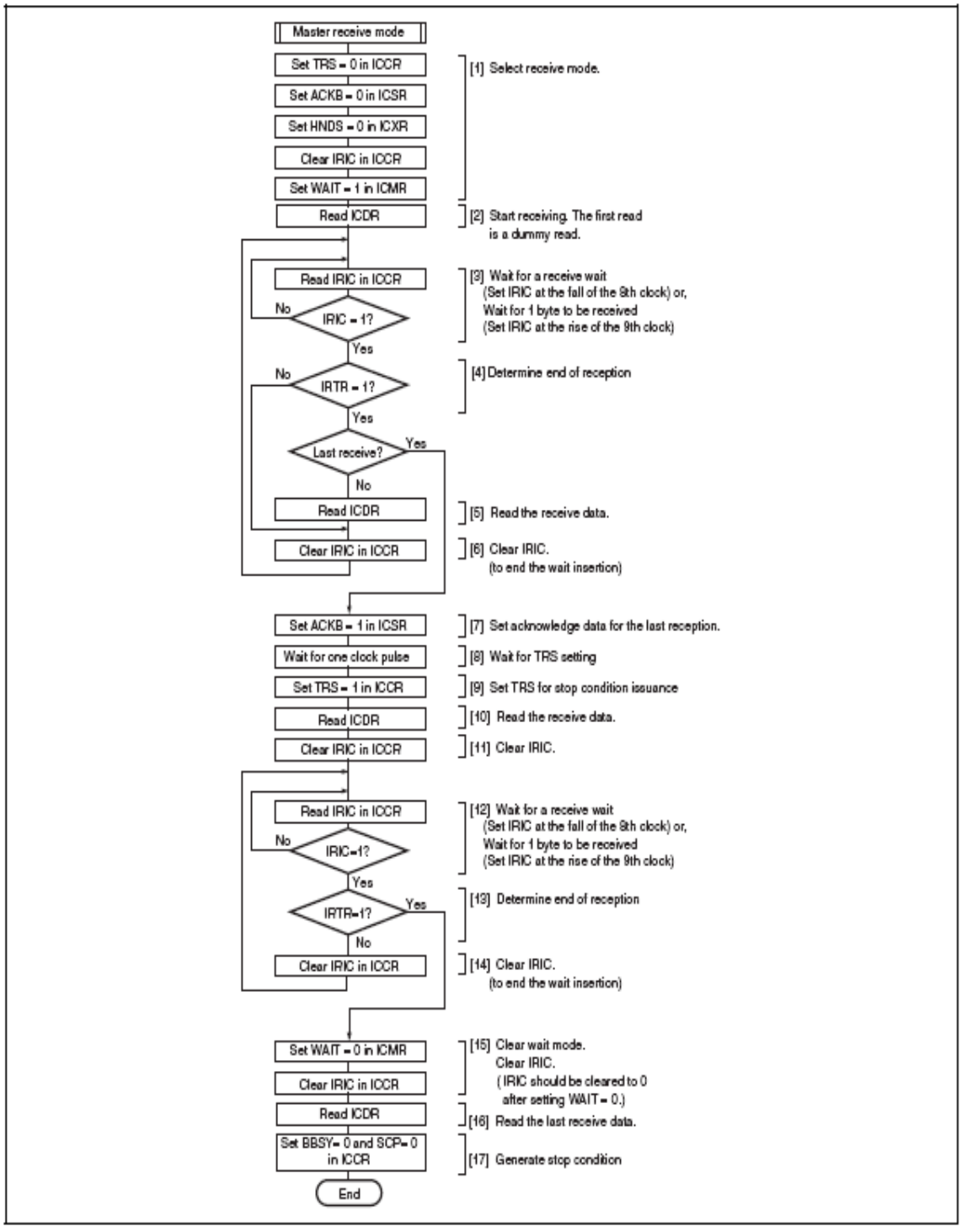

Figure 6.12: Sample Flowchart for Operations in Master Receive Mode (receiving a single byte) (WAIT = 1)

The following describes the multiple-byte reception procedure. In single-byte reception, some steps of the following procedure are omitted. At this time, follow the procedure:

[1] Clear the TRS bit in ICCR to 0 to switch from transmit mode to receive mode.
Clear the ACKB bit in ICSR to 0 to set the acknowledge data.
Clear the HNDS bit in ICXR to 0 to cancel the handshake function.
Clear the IRIC flag to 0, and then set the WAIT bit in ICMR to 1.

[2] When ICDR is read (dummy data is read), reception is started, and the receive clock is output, and data received, in synchronization with the internal clock.

[3] The IRIC flag is set to 1 in either of the following cases. If the IEIC bit in ICCR has been set to 1, an interrupt request is sent to the CPU.
(1) At the fall of the 8th receive clock pulse for one frame
SCL is automatically fixed low in synchronization with the internal clock until the IRIC flag clearing.
(2) At the rise of the 9th receive clock pulse for one frame
The IRTR and ICDRF flags are set to 1, indicating that one frame of data has been received. The master device outputs the receive clock continuously to receive the next data.

[4] Read the IRTR flag in ICSR.
If the IRTR flag is 0, execute step [6] to clear the IRIC flag to 0 to release the wait state.
If the IRTR flag is 1 and the next data is the last receive data, execute step [7] to halt reception.

[5] If IRTR flag is 1, read ICDR receive data.

[6] Clear the IRIC flag. When the flag is set as (1) in step [3], the master device outputs the 9th clock and drives SDA low at the 9th receive clock pulse to return an acknowledge signal.
Data can be received continuously by repeating steps [3] to [6].

[7] Set the ACKB bit in ICSR to 1 so as to return the acknowledge data for the last reception.

[8] After the IRIC flag is set to 1, wait for at least one clock pulse until the rise of the first clock pulse for the next receive data.

[9] Set the TRS bit in ICCR to 1 to switch from receive mode to transmit mode. The TRS bit value becomes valid when the rising edge of the next 9th clock pulse is input.

[10] Read the ICDR receive data.

[11] Clear the IRIC flag to 0.

[12] The IRIC flag is set to 1 in either of the following cases.
(1) At the fall of the 8th receive clock pulse for one frame
SCL is automatically fixed low in synchronization with the internal clock until the IRIC flag is cleared.
(2) At the rise of the 9th receive clock pulse for one frame
The IRTR and ICDRF flags are set to 1, indicating that one frame of data has been received.

[13] Read the IRTR flag in ICSR.
If the IRTR flag is 0, execute step [14] to clear the IRIC flag to 0 to release the wait state.
If the IRTR flag is 1 and data reception is complete, execute step [15] to issue the stop condition.

[14] If IRTR flag is 0, clear the IRIC flag to 0 to release the wait state.
Execute step [12] to read the IRIC flag to detect the end of reception.

[15] Clear the WAIT bit in ICMR to cancel the wait mode.
Clearing of the IRIC flag should be done while WAIT = 0. (If the WAIT bit is cleared to 0 after clearing the IRIC flag and then an instruction to issue a stop condition is executed, the stop condition may not be issued correctly.)

[16] Read the last ICDR receive data.

[17] Clear the BBSY bit and SCP bit to 0 in ICCR. This changes SDA from low to high when SCL is high, and generates the stop condition.

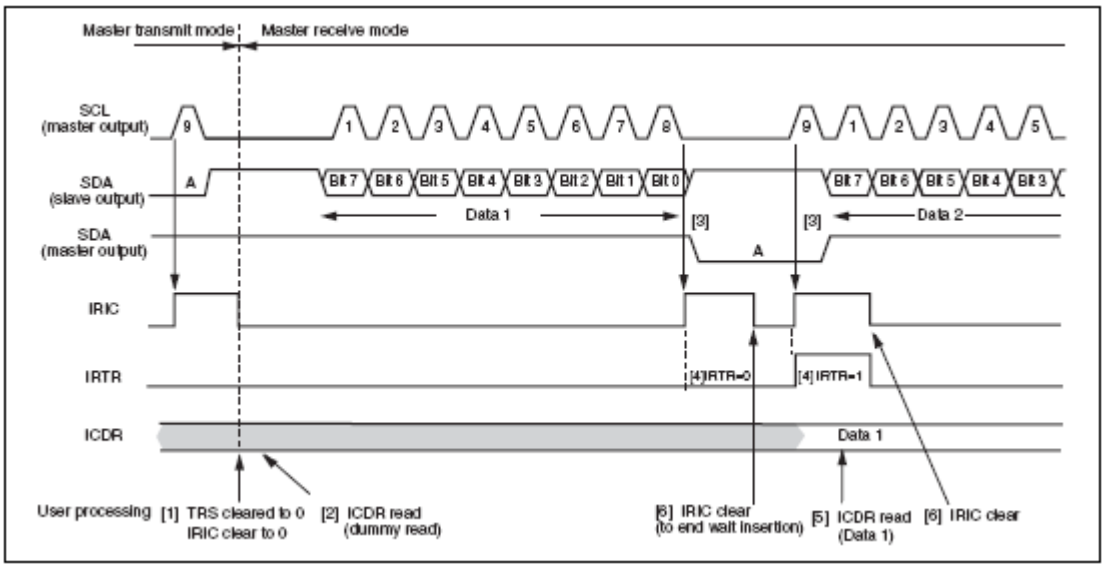

Figure 6.13: Master Receive Mode Operation Timing Example

(MLS = ACKB = 0, WAIT = 1)

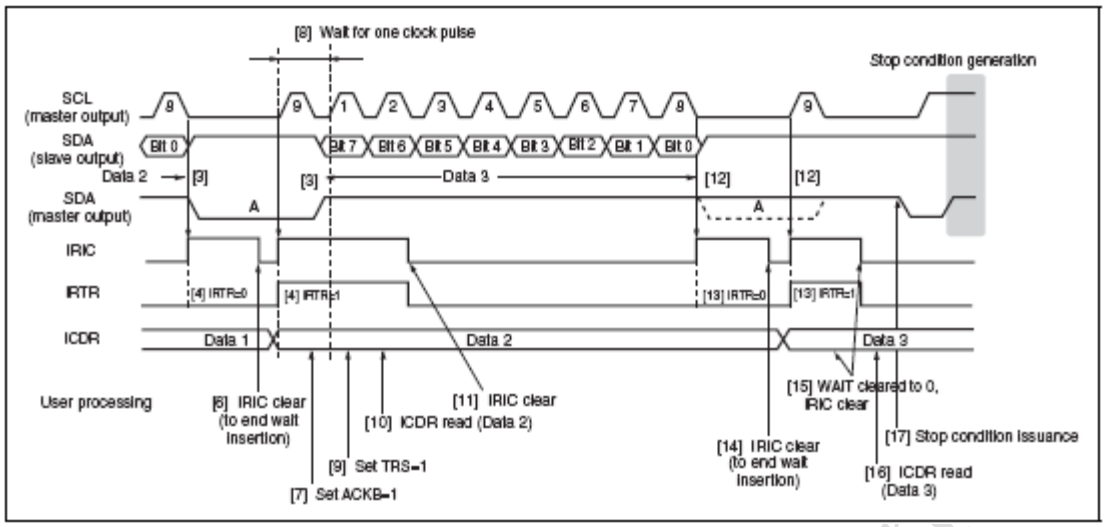

Figure 6.14: Stop Condition Issuance Timing Example in Master Receive Mode (MLS = ACKB = 0, WAIT = 1)

6.5 Slave Transmit Operation

In I^2C bus format slave receive mode:

- The master device outputs the transmit clock and transmit data
- The slave device returns an acknowledge signal

The slave device operates as the device specified by the master device when the slave address in the first frame following the start condition that is issued by the master device matches its own address.

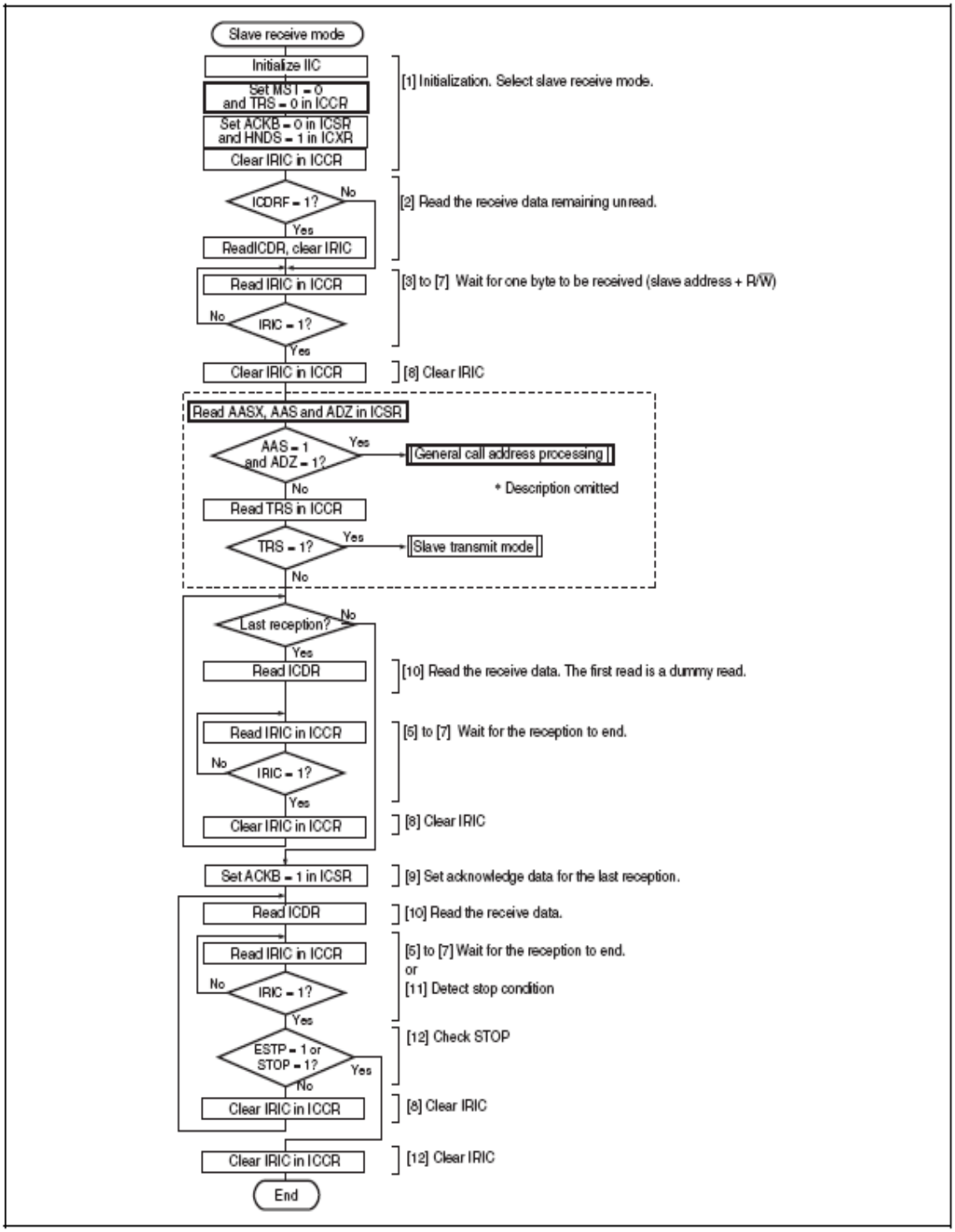

Figure 6.15: Sample Flowchart for Operations in Salve Receive Mode

(HNDS = 1)

The reception procedure and operations using the HNDS bit function by which data reception process is provided in 1-byte unit which SCL being fixed low at every data reception, are described below:

[1] Initialize the IIC as described in section 15.4.2, Initialization.

Clear the MST and TRS bits to 0 to set slave receive mode, and set the HNDS bit to 1 and the ACKB bit to 0. Clear the IRIC flag in ICCR to 0 to see the end of reception.

[2] Confirm that the ICDRF flag is 0. If the ICDRF flag is set to 1, read the ICDR and then clear the IRIC flag to 0.

[3] When the start condition output by the master device is detected, the BBSY flag in ICCR is set to 1. The master device then outputs the 7-bit slave address, and transmit/receive direction (R/$\overline{W}$), in synchronization with the transmit clock pulses.

[4] When the slave address matches in the first frame following the start condition, the device operates as the slave device specified by the master device. If the 8th data bit (R/$\overline{W}$) is 0, the TRS bit remains cleared to 0, and slave receive operation is performed. If the 8th data bit (R/$\overline{W}$) is 1, the TRS bit is set to 1, and slave transmit operation is performed. When the slave address does not match, receive operation is halted until the next start condition is detected.

[5] At the 9th clock pulse of the receive frame, the slave device returns the data in the ACKB bit as the acknowledge data.

[6] At the rise of the 9th clock pulse, the IRIC flag is set to 1. If the IEIC bit has been set to 1, an interrupt request is sent to the CPU.

If the AASX bit has been set to 1, IRTR flag is also set to 1.

[7] At the rise of the 9th clock pulse, the receive data is transferred from ICDRS to ICDRR, setting the ICDRF flag to 1. The slave device drives SCL low from the fall of the 9th receive clock pulse until data is read from ICDR.

[8] Confirm that the STOP bit is cleared to 0, and clear the IRIC flag to 0.

[9] If the next frame is the last receive frame, set the ACKB bit to 1.

[10] If ICDR is read, the ICDRF flag is cleared to 0, releasing the SCL bus line. This enables the master device to transfer the next data.

Receive operations can be performed continuously by repeating steps [5] to [10].

[11] When the stop condition is detected (SDA is changed from low to high when SCL is high), the BBSY flag is cleared to 0 and the STOP bit is set to 1. If the STOPIM bit has been cleared to 0, the IRIC flag is set to 1.

[12] Confirm that the STOP bit is set to 1, and clear the IRIC flag to 0.

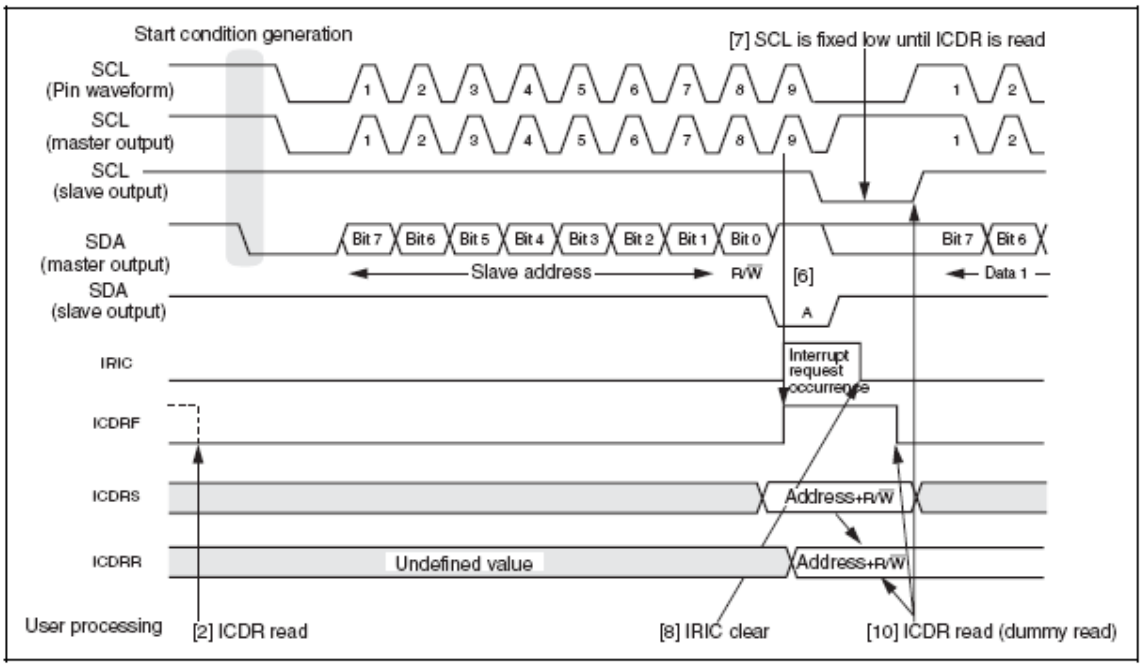

Figure 6.16: Slave Receive Mode Operation Timing Example (1)

(MLS = 0, HNDS = 1)

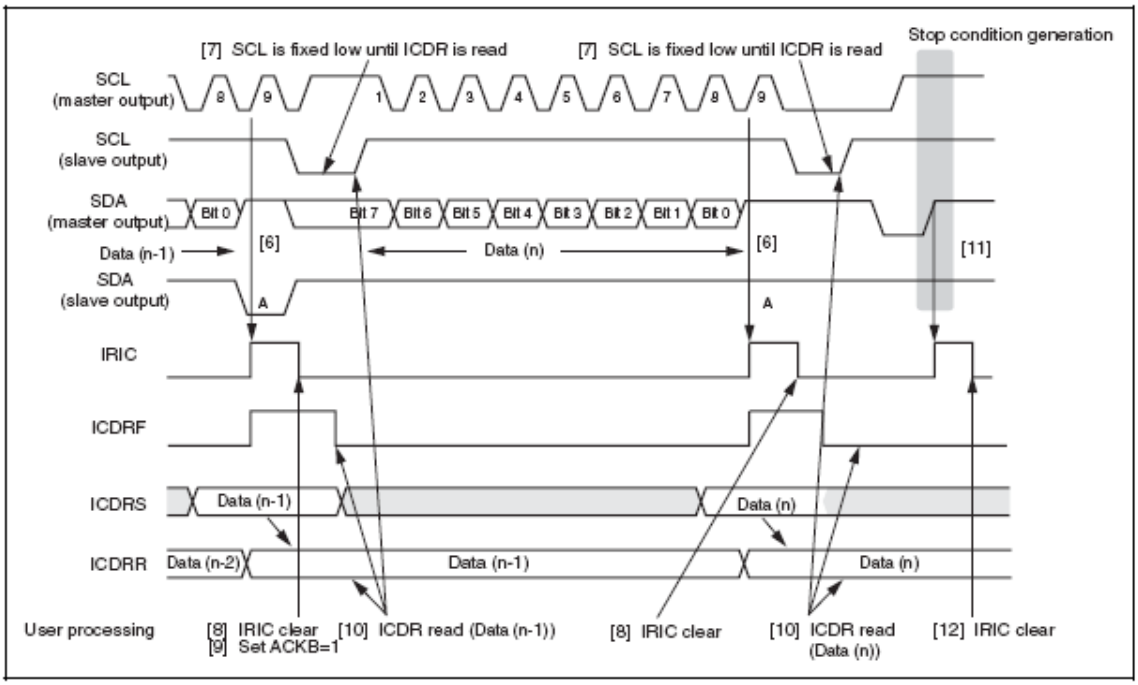

Figure 6.17: Slave Receive Mode Operation Timing Example (2)

(MLS = 0, HNDS = 1)

Continuous Receive Operation

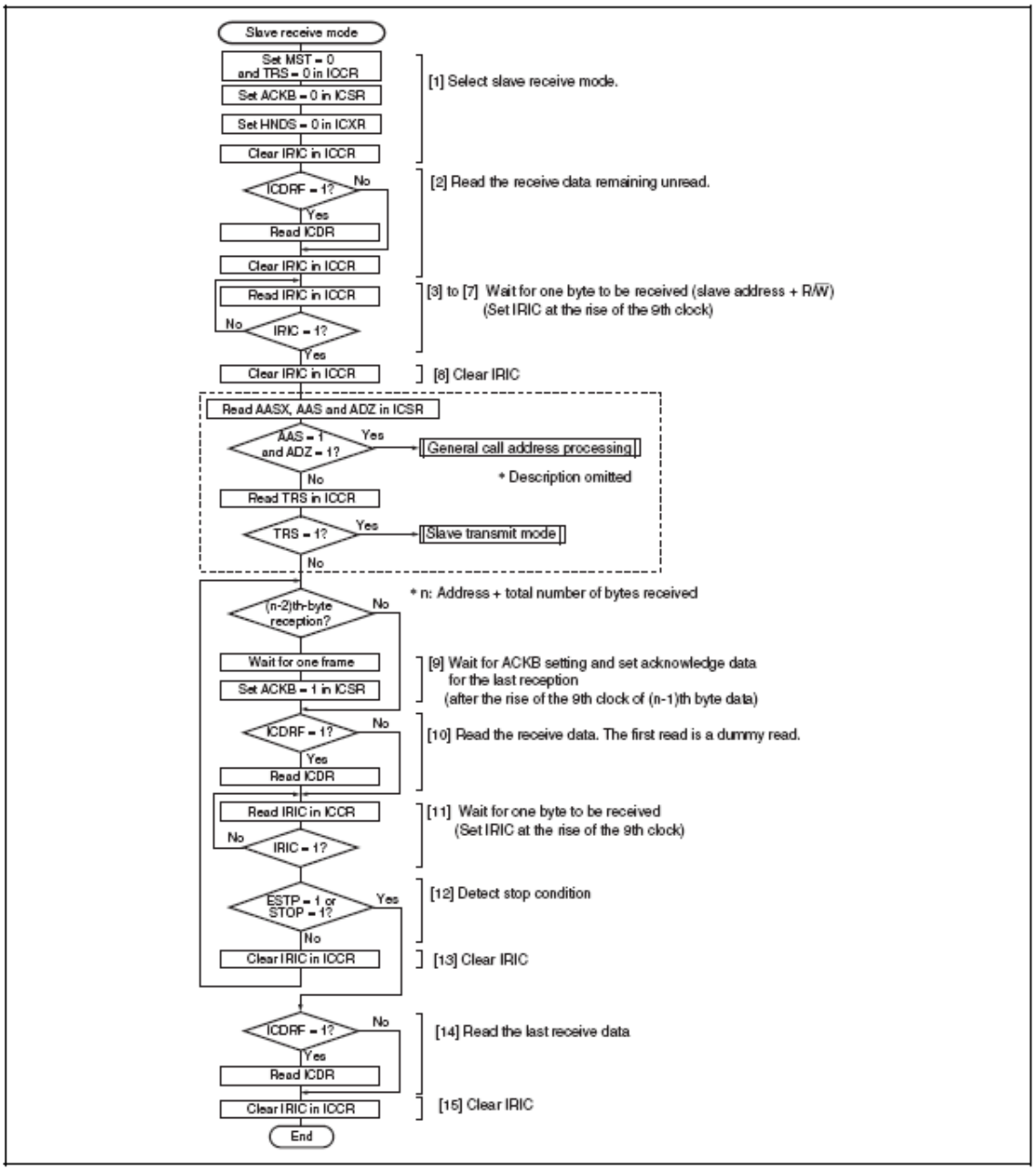

Figure 6.18: Sample Flowchart for Operations in Slave Receive Mode

(HNDS = 0)

[1] Initialize the IIC as described in section 15.4.2, Initialization.

Clear the MST and TRS bits to 0 to set slave receive mode, and set the HNDS and ACKB bits to 0. Clear the IRIC flag in ICCR to 0 to see the end of reception.

[2] Confirm that the ICDRF flag is 0. If the ICDRF flag is set to 1, read the ICDR and then clear the IRIC flag to 0.

[3] When the start condition output by the master device is detected, the BBSY flag in ICCR is set to 1. The master device then outputs the 7-bit slave address, and transmit/receive direction (R/W) in synchronization with the transmit clock pulses.

[4] When the slave address matches in the first frame following the start condition, the device operates as the slave device specified by the master device. If the 8th data bit (R/$\overline{W}$) is 0, the TRS bit remains cleared to 0, and slave receive operation is performed. If the 8th data bit (R/$\overline{W}$) is 1, the TRS bit is set to 1, and slave transmit operation is performed. When the slave address does not match, receive operation is halted until the next start condition is detected.

[5] At the 9th clock pulse of the receive frame, the slave device returns the data in the ACKB bit as the acknowledge data.

[6] At the rise of the 9th clock pulse, the IRIC flag is set to 1. If the IEIC bit has been set to 1, an interrupt request is sent to the CPU.

If the AASX bit has been set to 1, the IRTR flag is also set to 1.

[7] At the rise of the 9th clock pulse, the receive data is transferred from ICDRS to ICDRR, setting the ICDRF flag to 1.

[8] Confirm that the STOP bit is cleared to 0 and clear the IRIC flag to 0.

[9] If the next read data is the third last receive frame, wait for at least one frame time to set the ACKB bit. Set the ACKB bit after the rise of the 9th clock pulse of the second last receive frame.

[10] Confirm that the ICDRF flag is set to 1 and read ICDR. This clears the ICDRF flag to 0.

[11] At the rise of the 9th clock pulse or when the receive data is transferred from IRDRS to ICDRR due to ICDR read operation, The IRIC and ICDRF flags are set to 1.

[12] When the stop condition is detected (SDA is changed from low to high when SCL is high), the BBSY flag is cleared to 0 and the STOP or ESTP flag is set to 1. If the STOPIM bit has been cleared to 0, the IRIC flag is set to 1. In this case, execute step [14] to read the last receive data.

[13] Clear the IRIC flag to 0.

Receive operations can be performed continuously by repeating steps [9] to [13].

[14] Confirm that the ICDRF flag is set to 1, and read ICDR.

[15] Clear the IRIC flag.

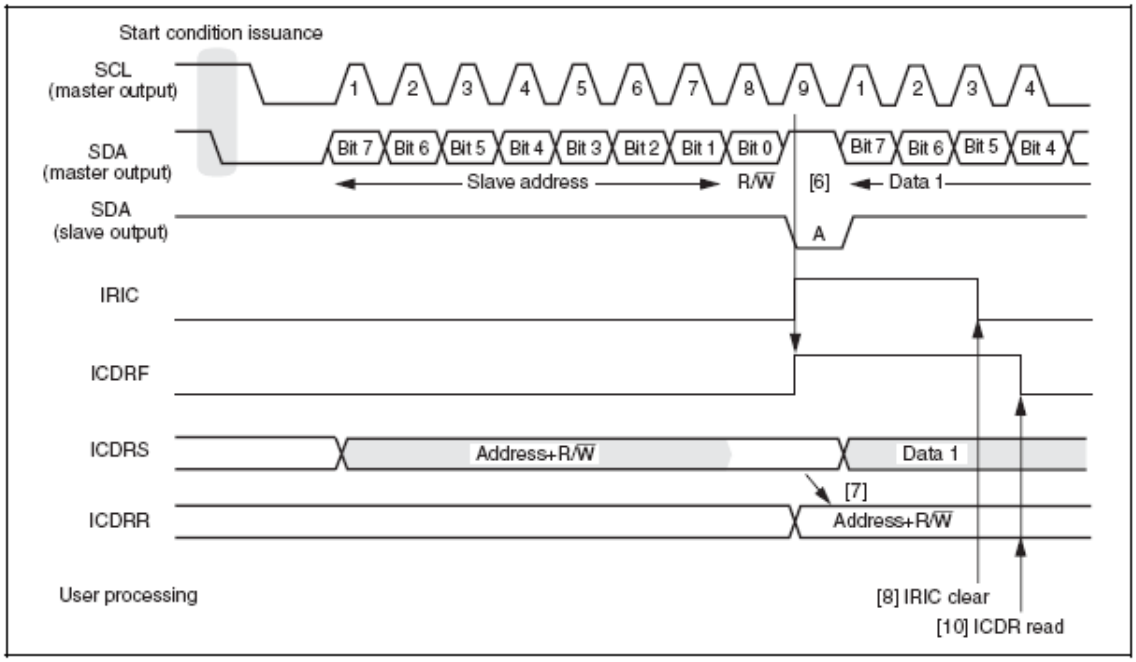

Figure 6.19: Slave Receive Mode Operation Timing Example (1)

(MLS = ACKB = 0, HNDS = 0)

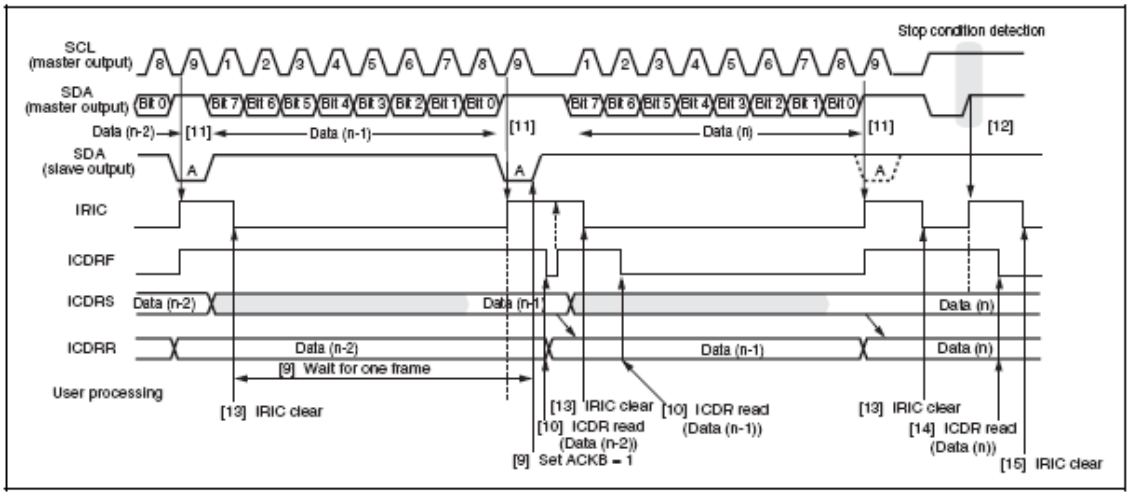

Figure 6.20: Slave Receive Mode Operation Timing Example (2)

(MLS = ACKB = 0, HNDS = 0)

6.6 Slave Transmit Operation

If the slave address matches to the address in the first frame (address reception frame) following the start condition detection when the 8th $(R/\overline{W})$ bit data is 1 (read), the TRS bit in ICCR is automatically set to 1 and the mode changes to slave transmit mode.

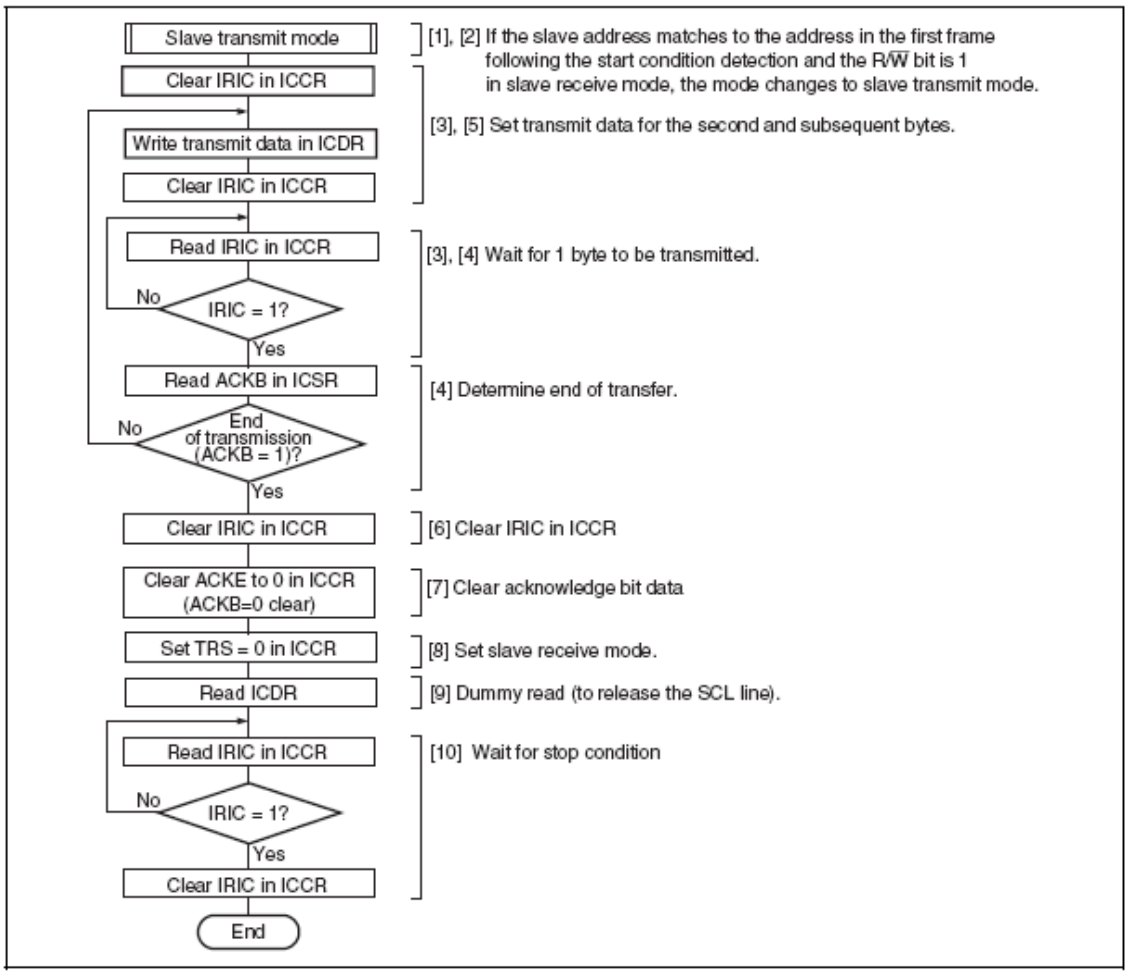

Figure 6.21: Sample Flowchart for Slave Transmit Mode

The transmission procedure and operation in slave transmit mode are described below:

[1] Initialize slave receive mode and wait for slave address reception.

[2] When the slave address matches in the first frame following detection of the start condition, the slave device drives SDA low at the 9th clock pulse and returns an acknowledge signal. If the 8th data bit (R/$\overline{W}$) is 1, the TRS bit in ICCR is set to 1, and the mode changes to slave transmit mode automatically. The IRIC flag is set to 1 at the rise of the 9th clock. If the IEIC bit in ICCR has been set to 1, an interrupt request is sent to the CPU. At the same time, the ICDRE flag is set to 1. The slave device drives SCL low from the fall of the 9th transmit clock until ICDR data is written, to disable the master device to output the next transfer clock.

[3] After clearing the IRIC flag to 0, write data to ICDR. At this time, the ICDRE flag is cleared to 0. The written data is transferred to ICDRS, and the ICDRE and IRIC flags are set to 1 again. The slave device sequentially sends the data written into ICDRS in accordance with the clock output by the master device.

The IRIC flag is cleared to 0 to detect the end of transmission. Processing from the ICDR register writing to the IRIC flag clearing should be performed continuously. Prevent any other interrupt processing from being inserted.

[4] The master device drives SDA low at the 9th clock pulse, and returns an acknowledge signal. As this acknowledge signal is stored in the ACKB bit in ICSR, this bit can be used to determine whether the transfer operation was performed successfully. When one frame of data has been transmitted, the IRIC flag in ICCR is set to 1 at the rise of the 9th transmit clock pulse. When the ICDRE flag is 0, the data written into ICDR is transferred to ICDRS and the ICDRE and IRIC flags are set to 1 again. If the ICDRE flag has been set to 1, this slave device drives SCL low from the fall of the 9th transmit clock until data is written to ICDR.

[5] To continue transmission, write the next data to be transmitted into ICDR. The ICDRE flag is cleared to 0. The IRIC flag is cleared to 0 to detect the end of transmission. Processing from the ICDR register writing to the IRIC flag clearing should be performed continuously. Prevent any other interrupt processing from being inserted.

Transmit operations can be performed continuously by repeating steps [4] and [5].

[6] Clear the IRIC flag to 0.

[7] To end transmission, clear the ACKE bit in the ICCR register to 0, to clear the acknowledge bit stored in the ACKB bit to 0.

[8] Clear the TRS bit to 0 for the next address reception, to set slave receive mode.

[9] Dummy-read ICDR to release SCL on the slave side.

[10] When the stop condition is detected, that is, when SDA is changed from low to high when SCL is high, the BBSY flag in ICCR is cleared to 0 and the STOP flag in ICSR is set to 1. When the STOPIM bit in ICXR is 0, the IRIC flag is set to 1. If the IRIC flag has been set, it is cleared to 0.

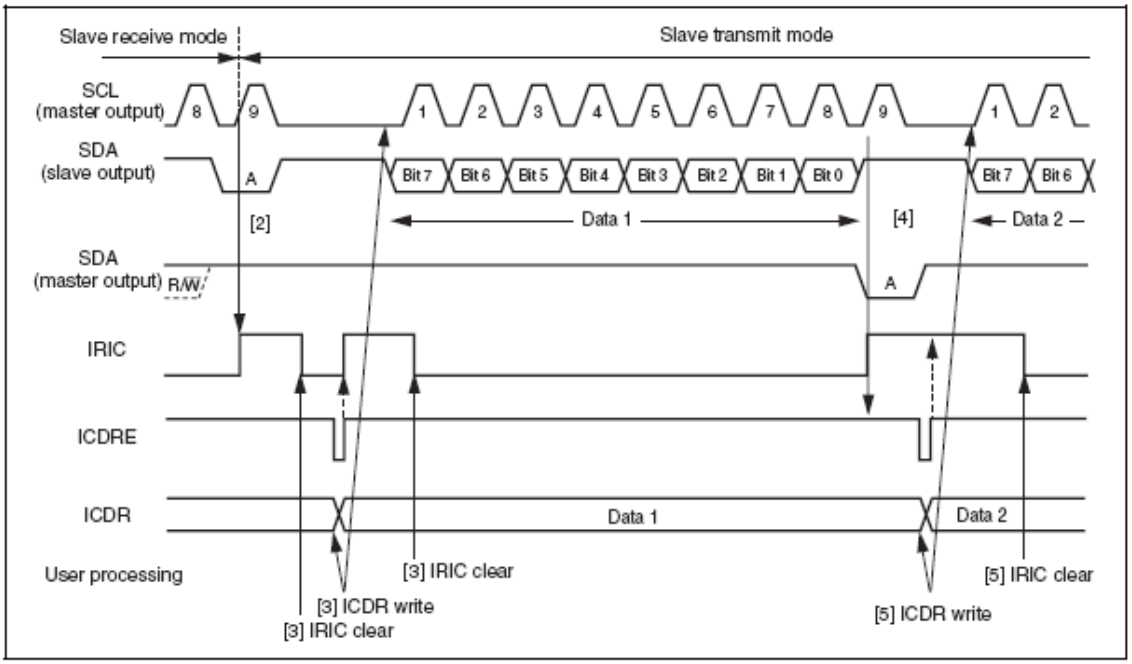

Figure 6.22: Slave Transmit Mode Operation Timing Example (MLS = 0)

6.7 IRIC Setting Timing and SCL Control

The interrupt request flag (IRIC) is set at different times depending on the WAIT bit in ICMR, the FS bit in SAR, and the FSX bit in SARX.

If the ICDRE or ICDRF flag is set to 1, SCL is automatically held low after one frame has been transferred; this timing is synchronized with the internal clock.

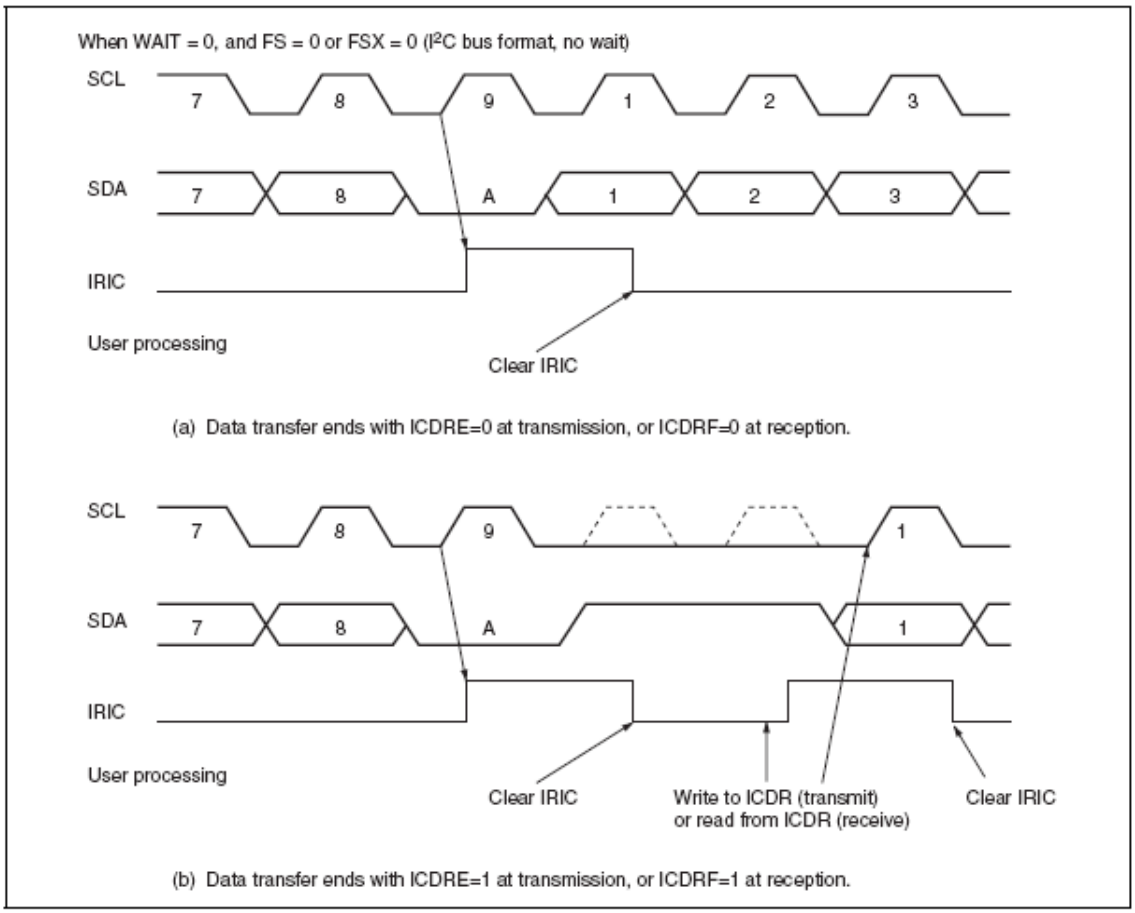

Figure 6.23: IRIC Setting Timing and SCL Control (1)

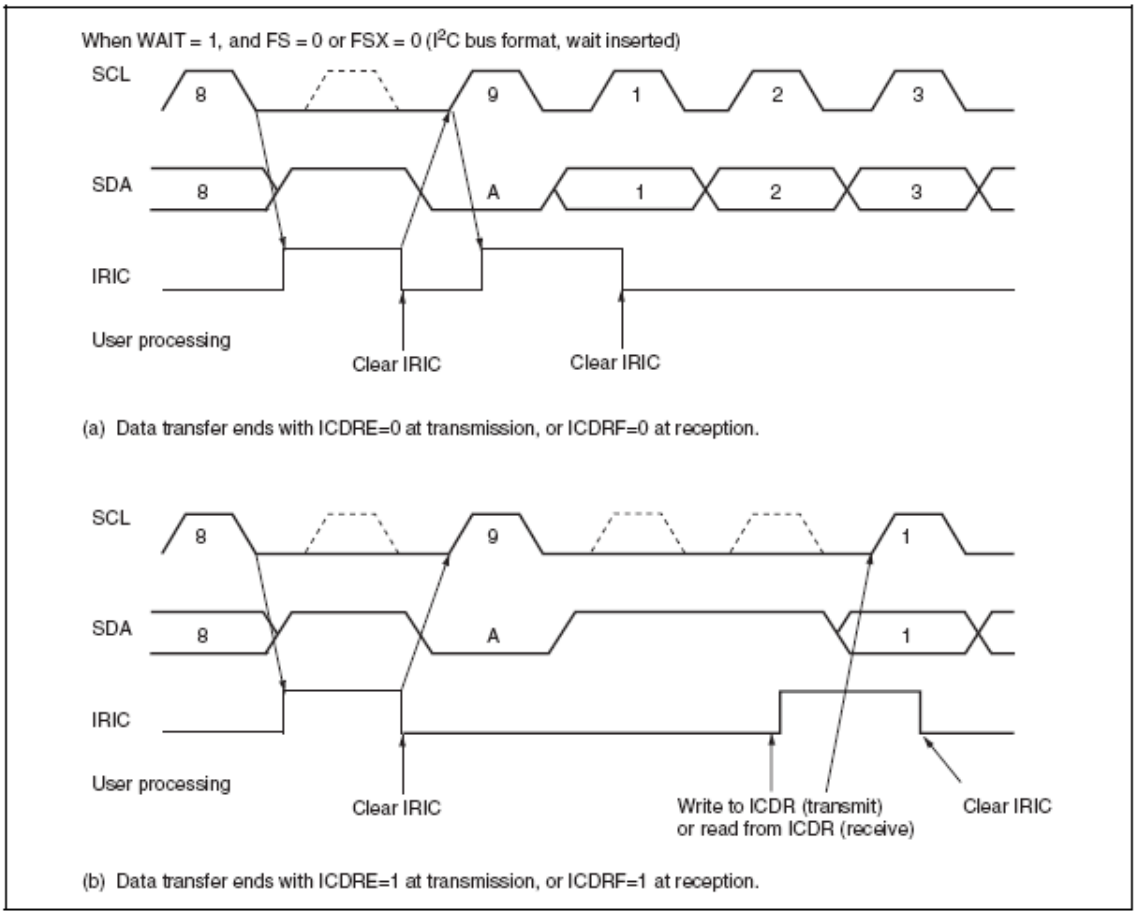

Figure 6.24: IRIC Setting Timing and SCL Control (2)

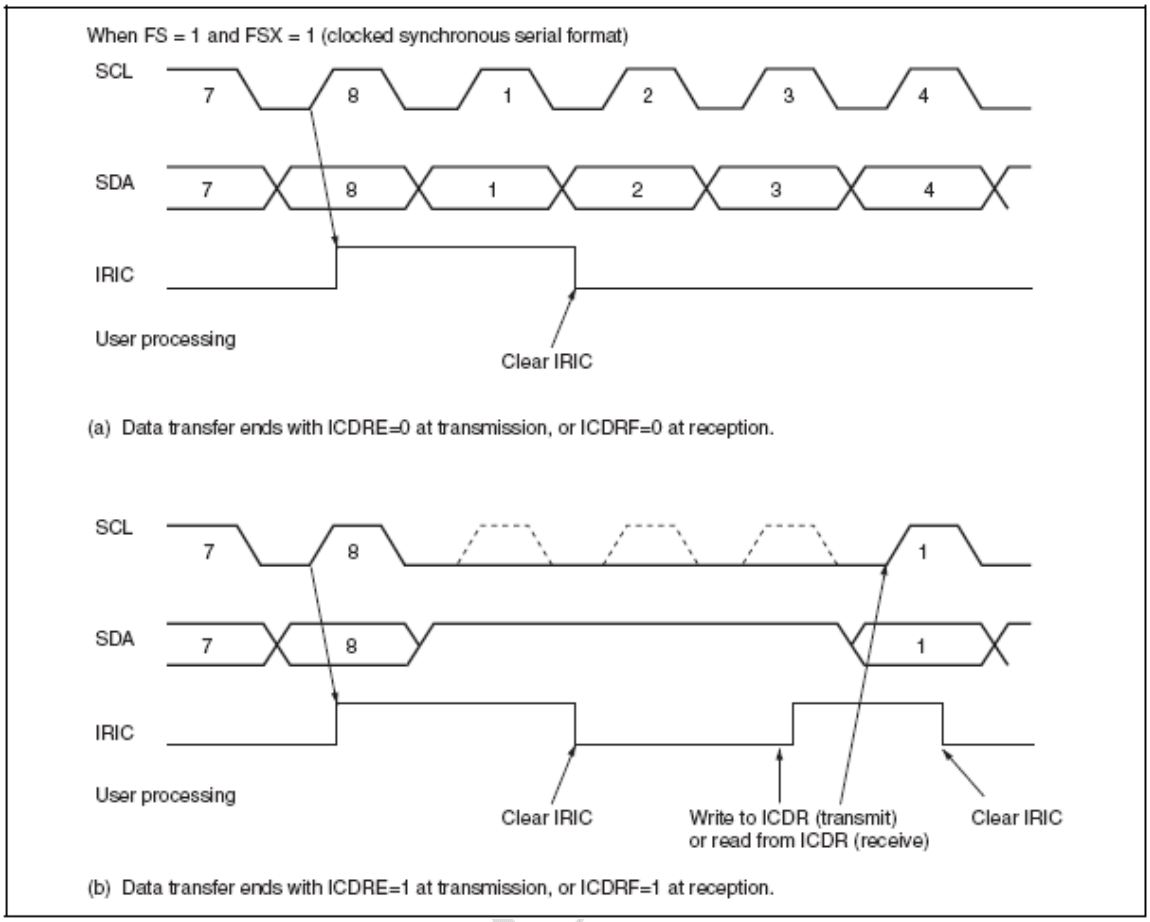

Figure 6.25: IRIC Setting Timing and SCL Control (3)

6.8 Operation Using the DTC

Item	Master Transmit Mode	Master Receive Mode	Slave Transmit Mode	Slave Receive Mode
Slave address + R/$\overline{W}$ bit transmission/ reception	Transmission by DTC (ICDR write)	Transmission by CPU (ICDR write)	Reception by CPU (ICDR read)	Reception by CPU (ICDR read)
Dummy data read	—	Processing by CPU (ICDR read)	—	—
Actual data transmission/ reception	Transmission by DTC (ICDR write)	Reception by DTC (ICDR read)	Transmission by DTC (ICDR write)	Reception by DTC (ICDR read)
Dummy data (H'FF) write	—	—	Processing by DTC (ICDR write)	—
Last frame processing	Not necessary	Reception by CPU (ICDR read)	Not necessary	Reception by CPU (ICDR read)
Transfer request processing after last frame processing	1st time: Clearing by CPU 2nd time: Stop condition issuance by CPU	Not necessary	Automatic clearing on detection of stop condition during transmission of dummy data (H'FF)	Not necessary
Setting of number of DTC transfer data frames	Transmission: Actual data count + 1 (+1 equivalent to slave address + R/$\overline{W}$ bits)	Reception: Actual data count	Transmission: Actual data count + 1 (+1 equivalent to dummy data (H'FF))	Reception: Actual data count

Figure 6.26: Examples of the Operation using DTC

6.9 Noise Canceller

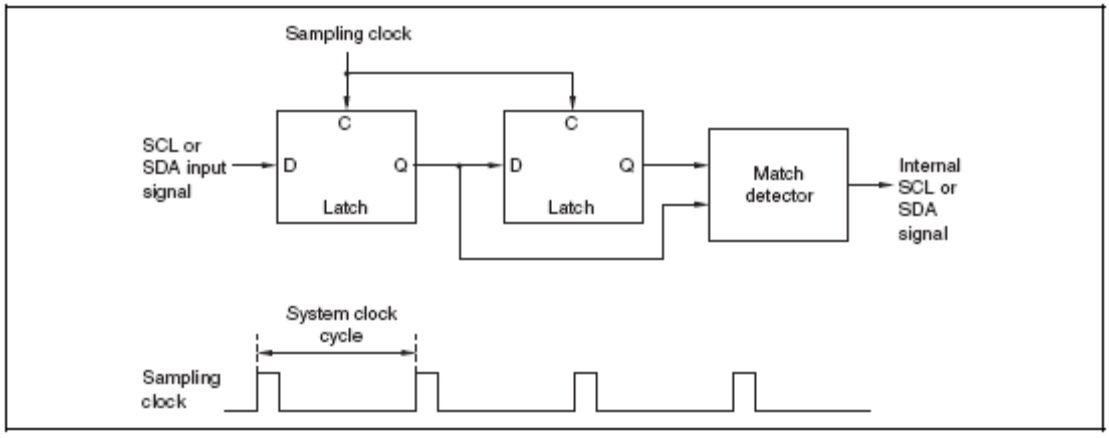

Figure 6.27: Block Diagram of Noise Canceller

6.10 Initialization of Internal State

Initialization is executed in accordance with clearing ICE bit.

Scope of Initialization: the initialization executed by this function covers the following items:

- ICDRE and ICDRF internal flags.
- Transmit/receive sequencer and internal operating clock counter.
- Internal latches for retaining the output state of the SCL and SDA pins (wait, clock, data, output…).

The following items are not initialized:

- Actual register values (ICDR, SAR, SARX, ICMR, ICCR, ICSR, ICXR (other than ICDRE and ICDRF)).
- Internal latches used to retain register read information for setting/clearing flags in the ICMR, ICCR and ICSR registers.
- The value of the ICMR register bit counter (BC2 to BC0).
- Generated interrupt sources (interrupt sources transferred to the interrupt controller).

To prevent problems caused by these factor, the following procedure should be used when initializing the IIC state:

- Execute initialization of the internal state according to the ICE bit clearing.
- Execute a stop condition issuance instruction (write 0 to BBSY and SCP) to clear the BBSY bit to 0 and wait for two transfer rate clock cycles.
- Re-execute initialization of the internal state according to the ICE bit clearing.
- Initialize (reset) the IIC registers.

-End-