
YOVI 2008 Core

Serial Communication Interface (SCIA)

Function Specifications

Rev 0.00

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1. Scope

This document is the Function Specifications of SCIA module for YOVI 2008 Core.

2. Feature

Serial Communication Interface (SCIA) perform synchronous serial transfer of 8-bit or 16-bit data

- Choice of 8-bit or 16-bit data length
- Choice of eight internal clock sources ($\Phi/1024$, $\Phi/256$, $\Phi/128$, $\Phi/64$, $\Phi/32$, $\Phi/16$, $\Phi/8$, $\Phi/4$, $\Phi/2$) or an external clock
- Interrupt request at complete of transfer

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3. Block diagram of SCIA

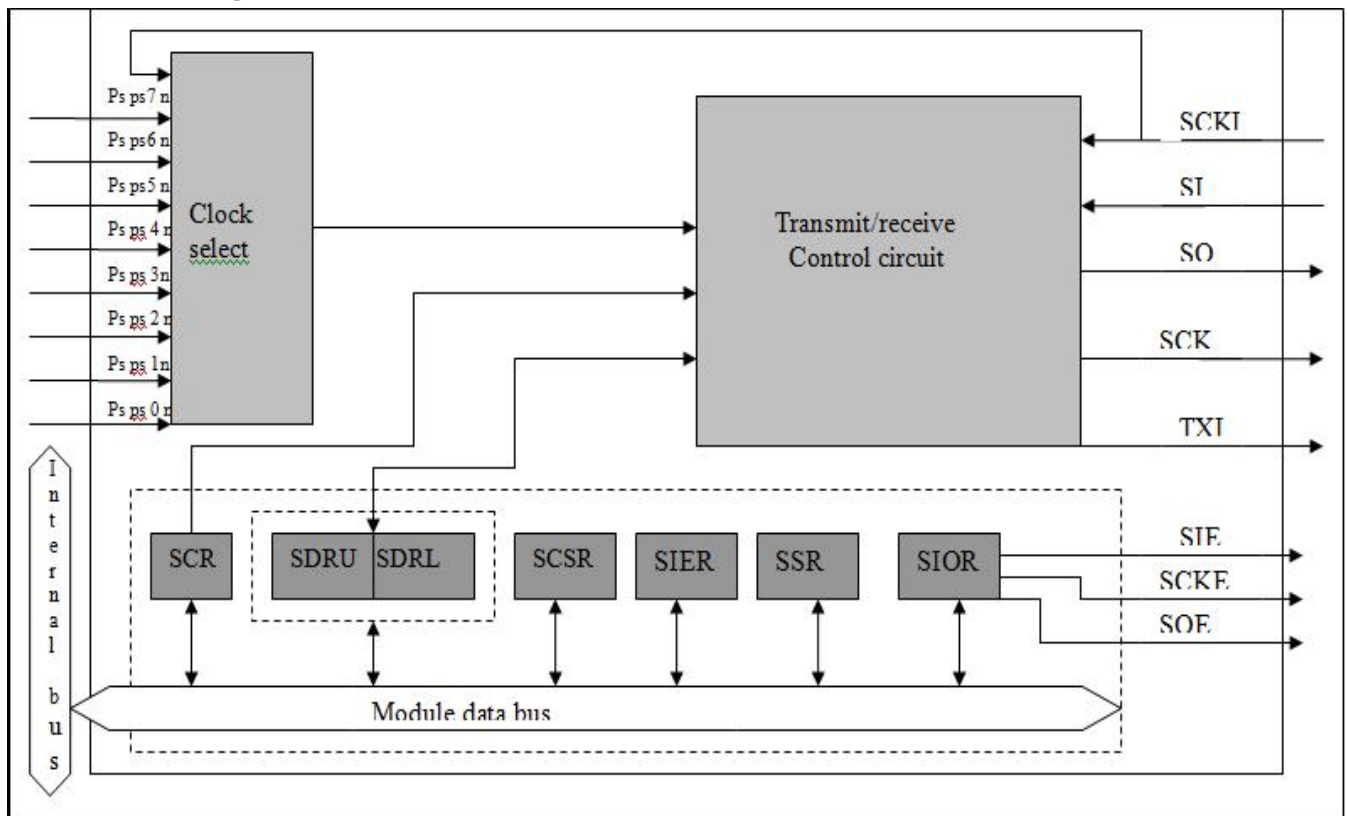


Figure 3.1: Block Diagram

Legend:

SCR:	Serial Control Register
SCSR:	Serial Control Status Register
SDRU:	Serial Data Register U
SDRL:	Serial Data Register L
SIOR:	Serial I/O control Register
SIER:	Serial Interrupt Enable Register
SSR:	Serial Status Register

4. Port Descriptions

Table 4.1 shows the SCIA port description.

Table 4.1 Port Descriptions

Name	I/O	Function
SCKI	Input	SCIA serial clock input
SCKO	Output	SCIA serial clock output
CKDIR	Output	SCIA serial clock direction control
SI	Input	SCIA receive data input
SO	Output	SCIA transmit data output
SCKOE	Output	SCIA serial clock output enable
SIE	Output	SCIA receive data input enable
SOE	Output	SCIA transmit data output enable

5. Register Descriptions

This SCIA module has the following registers:

- | | |
|--|----------------------|
| • Serial Control Register (SCR) | Relative address:H'0 |
| • Serial Control Status Register (SCSR) | Relative address:H'1 |
| • Serial Data Register Upper byte (SDRU) | Relative address:H'2 |
| • Serial Data Register Lower byte (SDRL) | Relative address:H'3 |
| • Serial I/O control Register (SIOR) | Relative address:H'4 |
| • Serial Interrupt Enable Register(SIER) | Relative address:H'5 |
| • Serial Status Register (SSR) | Relative address:H'6 |

5.1 Serial Control Register (SCR)

SCR is an 8-bit read/write register for selecting the operation mode and the prescaler division ratio

Upon reset, SCR is initialized to H'00. Writing to this register during a transfer stops the transfer.

Bit	7	6	5	4	3	2	1	0
	SNC1	SNC0	—	—	CKS3	CKS2	CKS1	CKS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	-	-	R/W	R/W	R/W	R/W

Bit	Bit name	Initial value	R/W	Description
7-6	SNC1-0	00	R/W	Operation mode select 00:8 bit synchronous transfer mode 01:16 bit synchronous transfer mode 10:Continuous clock output mode *1 11:Reserve *2
5-4	-	00	-	Reserved
3	CKS3	0	R/W	Select clock source 0:clock source is prescaler S (internal clock) 1:clock source is external clock
2-0	CKS2-0	000	R/W	Internal clock select 000: ps_ps9_n is selected ($\Phi/1024$) 001:ps_ps7_n is selected ($\Phi/256$) 010:ps_ps5_n is selected ($\Phi/64$) 011:ps_ps4_n is selected ($\Phi/32$) 100:ps_ps3_n is selected ($\Phi/16$) 101:ps_ps2_n is selected ($\Phi/8$) 110:ps_ps1_n is selected ($\Phi/4$) 111:ps_ps0_n is selected ($\Phi/2$)

Note: 1.In this mode ,transfer is not executed

2.Don't set bits SNC1 and SNC0 to "11"

5.2 Serial Control Status Register (SCSR)

SCSR is an 8-bit register indicating operation status, error status and setting the start command

Upon reset, SCSR is initialized to 0x9C. Writing to this register during a transfer stops the transfer

Bit	7	6	5	4	3	2	1	0
	-	SOL	ORER	-	-	-	-	STF
Initial value	1	0	0	1	1	1	0	0
Read/Write	-	R/W	R/W*	-	-	-	-	R/W

Note : *Only write of 0 for flag clearing is possible.

Bit	Bit name	Initial value	R/W	Description
7	-	1	-	Reserved
6	SOL	0	R/W	Extended data bit*1

SOL steps SO output level. When read, SOL returns the output level at the SO port.

0: SO output level is LOW (when read)

SO output level changes to LOW (when write)

1: SO output level changes is HIGH (when read)

SO output level changes to HIGH (when write)

5	ORER	0	R/W	<p>Overrun Error Flag</p> <p>ORER indicates the occurrence of an overrun error when an external clock is used. If a noise occurs after a transfer, causing an extraneous pulse to be superimpose on the normal serial clock, incorrect data may be transferred, then ORER is set to 1 to indicate an overrun.</p> <p>0: Clear condition</p> <p>After reading ORER = 1,cleared by writing 0 to ORER</p> <p>1:0 Setting condition</p> <p>Set if a clock pulse is input after a transfer in complete when an external clock is used</p>
4-1	-	1110	-	Reserved
0	STF	0	R/W	<p>Start Flag</p> <p>STF controls of a transfer. Setting this bit to 1 causes SCIA to start transfer data.</p> <p>0: Indicates that transfer is stopped (when read)</p> <p>Invalid(when write)</p> <p>1:Indicates transfer is in progress(when read)</p> <p>Start a transfer operation (when write)</p> <p>In continuous clock mode, this bit can not be set to 1</p>

Notes: 1 After completion of a transmission, SO continues to output the value of the last bit

Of transmitted data. The SO output can be changed by writing to SOL before or after

A transmission. The SOL bit setting remains valid only until the start of the next transmission. To control the level of the SO pin after transmission ends, it is necessary to write to the SOL bit at the end of each transmission. Do not write to this register while transmission is in progress, because that may cause a malfunction.

2 .During the transfer or while waiting for the first clock pulse, this bit remains set to 1. It is cleared to 0 upon completion of the transfer. It can therefore be use as a busy flag.

5.3 Serial Data Register Upper byte (SDRU)

SDRU is an 8-bit read/write register. It is used as the data register for the upper 8 bits In 16-bit transfer (SDRL in used for the lowest 8 bits).

Data written to SDRU is output or SDRL starting from the least significant bit (LSB). This data is then replaced by LSB-first data input at pin SI, which is shifted in the direction from the most significant bit (MSB) toward the LSB.

SDRU must be written or read only after data transmission or reception is complete. If this register is written or read while a data transfer is in progress, the data contents are not guaranteed.

The SDRU value upon reset is H'00.

Bit	7	6	5	4	3	2	1	0
	SDRU7	SDRU6	SDRU5	SDRU4	SDRU3	SDRU2	SDRU1	SDRU0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

5.4 Serial Data Register Lower byte (SDRL)

SDRL is an 8-bit read/write register. It is used as the data register in 8-bit transfer, and as the data register for the lower 8 bits in 16-bits transfer (SDRU is used for the upper 8 bits).

In 8-bits transfer, data written to SDRL is output from pin SO starting from the least significant bit (LSB). This data is then replaced by LSB-first data input at pin SI, which is shift in the direction from the most significant bit (MSB) toward the LSB.

In 16-bit transfer, operation is the same as for 8-bit transfer, except that input data is fed in via SDRU.

SDRL must be written or read only after data transmission or reception is complete. If this register is read or written while a data transfer is in progress, the data contents are not guaranteed.

SDRL value upon reset is H'00.

Bit	7	6	5	4	3	2	1	0
	SDRL7	SDRL6	SDRL5	SDRL4	SDRL3	SDRL2	SDRL1	SDRL0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

5.5 Serial I/O control Register (SIOR)

SIOR is an 8-bit read/write register, controlling the SI, SO and SCKO enable.

Upon reset, SIOR is initialized to H'00

Bit	7	6	5	4	3	2	1	0
	-	-	-	-	-	SDRL2	SDRL1	SDRL0
Initial value	0	0	0	0	0	0	0	0
Read/Write	-	-	-	-	-	R/W	R/W	R/W

Bit	Bit name	Initial value	R/W	Description
7-3	-	00000	-	reserved
2	SOE	0	R/W	Serial data output enable 0:SO disable 1:SO output enable
1	SIE	0	R/W	Serial data input enable 0:SI disable 1:SI input enable
0	SCKE	0	R/W	Serial clock output enable 0:SCKO disable 1:SCKO output enable

5.6 Serial Interrupt Enable Register (SIER)

SIER is an 8-bit read/write register that enable or disables interrupt requests.

Upon reset, SIER is initialized to H'00.

IEN can not written while interrupt signal IRR is still 1, this bit can be changed When IRR is cleared to 0

Bit	7	6	5	4	3	2	1	0
	-	-	-	IEN	-	-	-	-
Initial value	0	0	0	0	0	0	0	0
Read/Write	-	-	-	R/W	-	-	-	-

Bit	Bit name	Initial value	R/W	Description
7-5	-	000	-	Reserved
4	IEN	0	R/W	Interrupt request enable 0: interrupt request disables 1: interrupt request enables
3-0	-	0000	-	reserved

5.7 Serial Status Register (SSR)

SSR is an 8-bit read/written register , In which a corresponding flag is set to 1 when SCIA interrupt is request. The flag is not cleared automatically when an interrupt is accepted. It is necessary to write 0 to clear after reading 1. Upon reset , SSR is initialized to H'00.

Bit	7	6	5	4	3	2	1	0
	-	-	-	IRR	-	-	-	-
Initial value	0	0	0	0	0	0	0	0
Read/Write	-	-	-	R/W	-	-	-	-

Bit	Bit name	Initial value	R/W	Description
7-5	-	000	-	Reserved
4	IRR	0	R/W	Interrupt request flag 0: Clear condition When IRR=1,it is cleared by writing 0 after 1 1: Setting condition When a SCIA transfer is completed
3-0	-	0000	-	reserved

6 Operation

This SCIA has two types of operation. One is transfer operation (transmit/receive) and the other is continuous clock output operation.

In both operations, user can be select clock sources from 8 internal clocks and external clock.

6.1 Transmit

6.1.1 Internal clock

SCIA outputs SCKO and SO in this operation.

Data is sent in an 8-bit or 16-bit format, and starting from the least significant bit, in LSB-first format. Data is changed at the falling edge of SCKO.

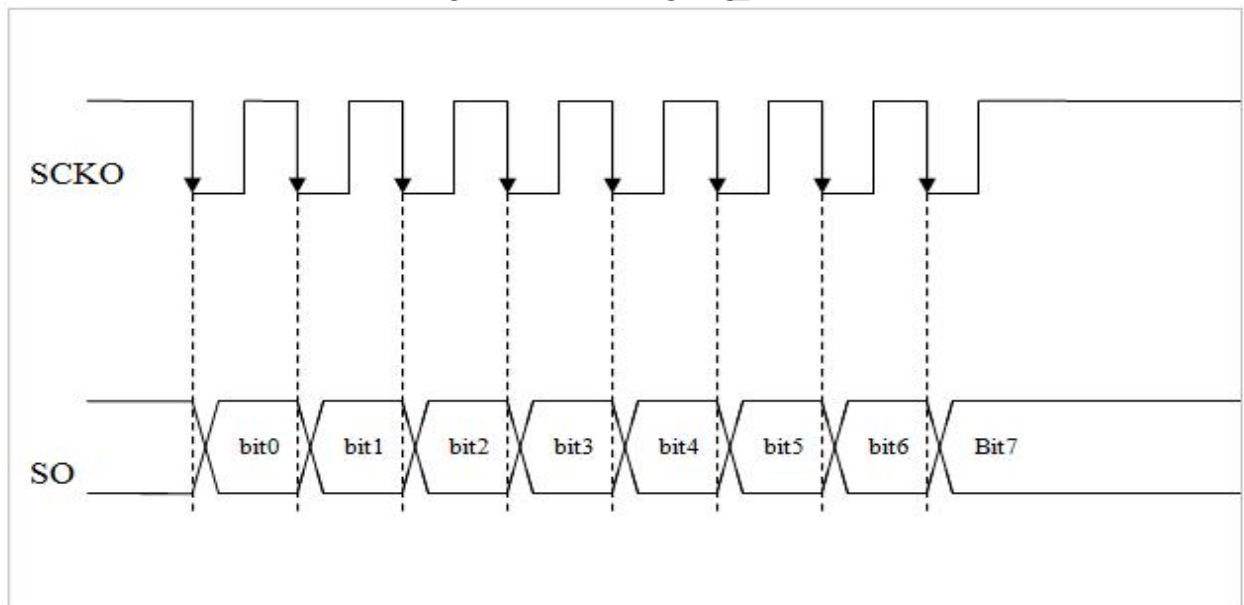


Figure 6.1 Transmit data format with internal clock

A transmitt operation is carried out as follows:

1. Set bits SOE, SCKE to 1 in SIOR to select SO and SCKO pin function.
2. Clear bits SNC1 and CKS3 in SCR to 0 and set bit SNC0 to 0 or 1, designating 8-bit or 16-bit synchronous transfer mode. Select the serial clock in bits CKS2 to CKS0.
3. Write transmit data in SDRL and SDRU as follows:
 8-bit transfer mode: SDRL
 16-bit transfer mode: Upper byte
4. Set the SCSR start flag (STF) to 1. SCIA starts operation and outputs transmit data at pin SO.
5. After data transmission is complete, bit IRR in SSR is set to 1.

A serial clock is output from pin SCKO in synchronization with the transmit data. After data transmission is complete, the serial clock is not output until the next time The start flag is set to 1. During this time, pin SO continues to output the value of the last transmitted bit.

While transmission is stop, the output value of pin SO can be changed by rewriting bit SOL in SCSR.

6.1.2 External clock

SCIA inputs SCKI and outputs SO in this operation.

Data is sent in a 8-bit or 16-bit format, and starting from the least significant bit, in LSB-first format. Data is change at the falling edge of SCKI.

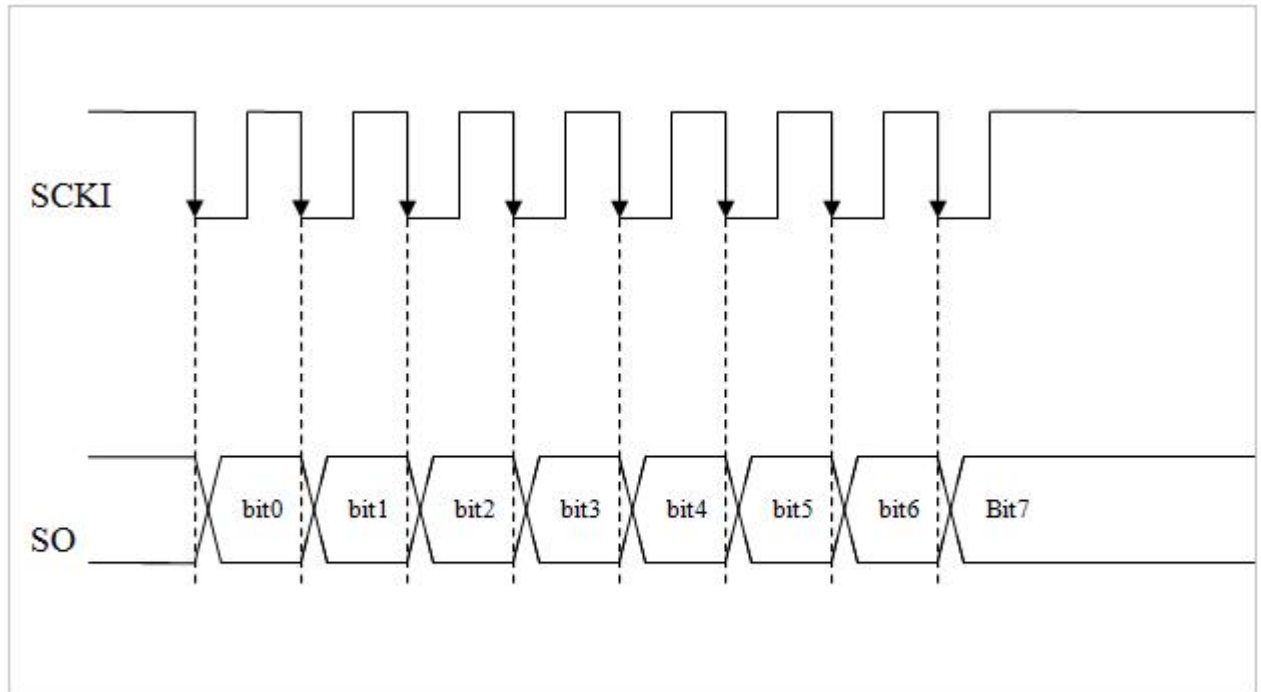


Figure 6.2. Transmit data format with clock

A transmit operation is carried out as follows:

1. Set bits SOE to 1 in SIOR to select SO pin functions.
2. Clear bit SNC1 in SCR to 0, set bit CKS3 in SCR to 1 and set bit SNC0 to 0 or 1, designating 8-bit or 16-bit synchronous transfer mode.
3. Write transmit data in SDRL and SDRU as follows:
8-bit transfer mode: SDRL
16-bit transfer mode: Upper byte
4. Set the SCSR start flag (STF) to 1. SCIA starts operation and outputs transmit data at pin SO.
5. After data transmission is complete, bit IRR in SSR is set to 1.

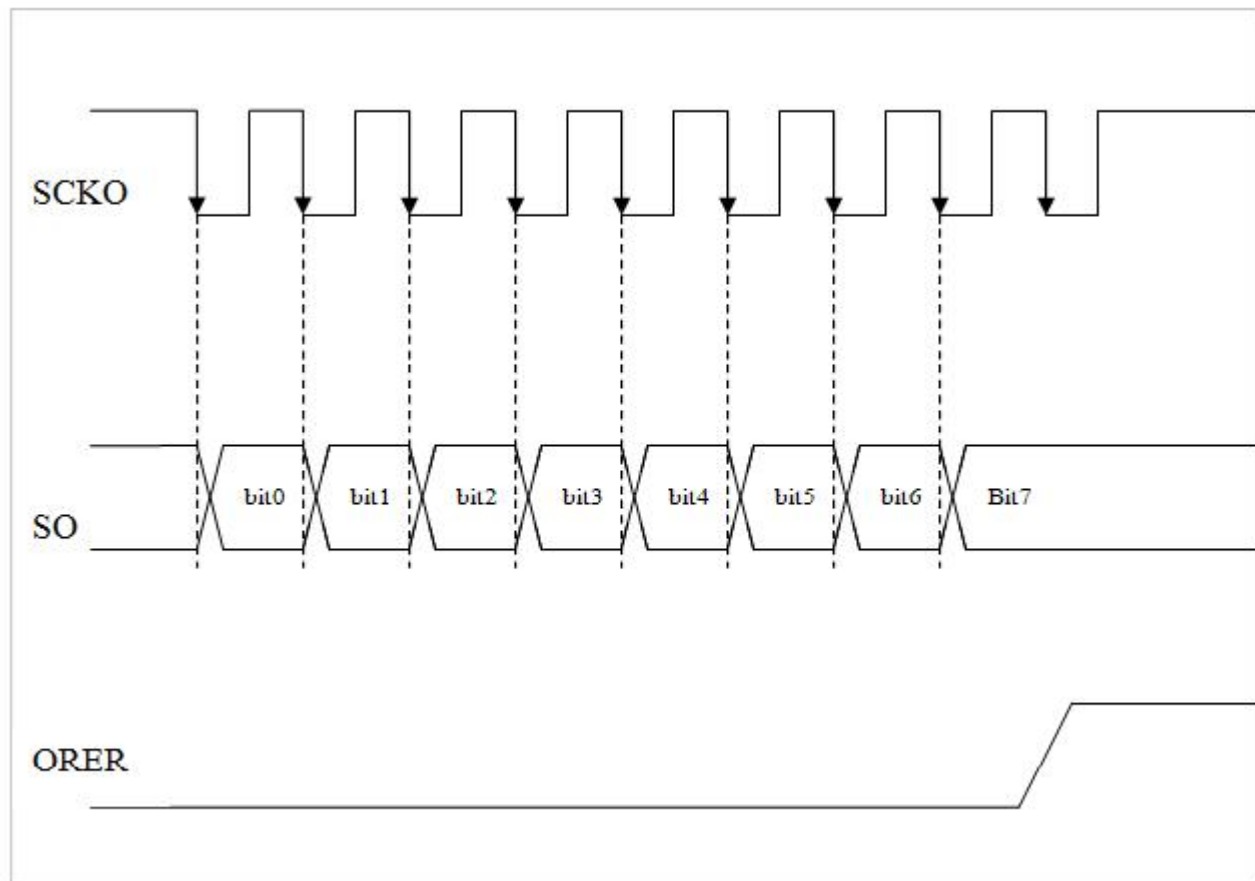


Figure 6.3 Overrun occurs in transmission with external clock

Data is transmitted in synchronization with the serial clock input at pin SCKI. After data transmission is complete, an overrun occurs if the serial clock continues to be input; no data is transmitted and the SCSR overrun flag (bit ORER) is set to 1.

During the time a transfer is complete, in IO continues to output the value of the last transmitted bit.

While transmission is stopped, the output value of pin SO can be change by rewriting bit SOL in SCSR.

6.2 Receive

6.2.1 Internal clock

SCIA outputs SCKO and inputs SI.

Data is received in an 8-bit or 16-bit format, and starting the least significant bit, in LSB-first format. SCIA captures SI at the rising edge of SCKO.

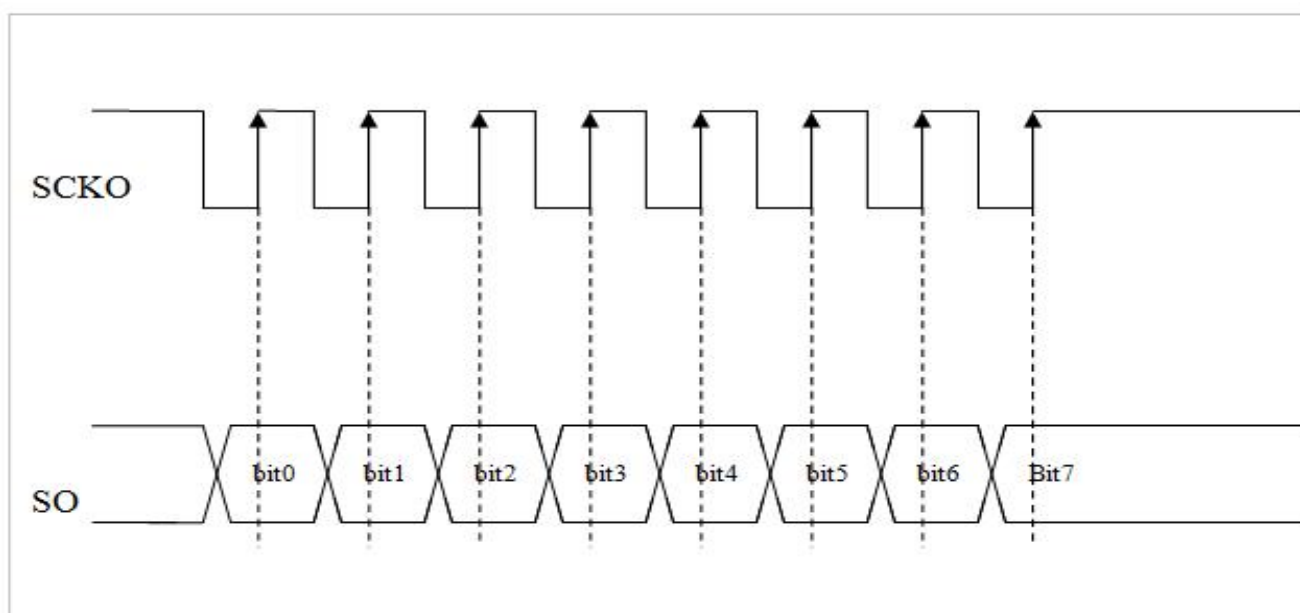


Figure 6.4 Receive data and capture timing with internal clock

A received operation is carried out of follows:

1. Set bits SIE and SCKE to 1 in SIOR to select the SI and SCKO pin function.
2. Clear bits SCN1 and CKS3 in SCR to 0 and set bit SNC0 to 0 or 1, designating 8-bit or 16-bit synchronous transfer mode. Select the serial clock in bits CKS2 to CKS0.
3. Set the SCSR start flag (STF) to 1. SCIA starts operation and receives data at pin SI.
4. After data reception is complete, bit IRR in SSR is set to 1.
5. Read the received data from SDRL, SDRU as follows:
 8-bit transfer mode: SDRL
 16-bit transfer mode: Upper byte in SDRU, lower byte in SDRL

6.2.2 External clock

SCIA inputs SI and SCKI.

Data is received in an 8-bit and 16-bit format, and starting from the least significant bit, in LSB-first format. SCIA captures SI at the rising edge SCKI.

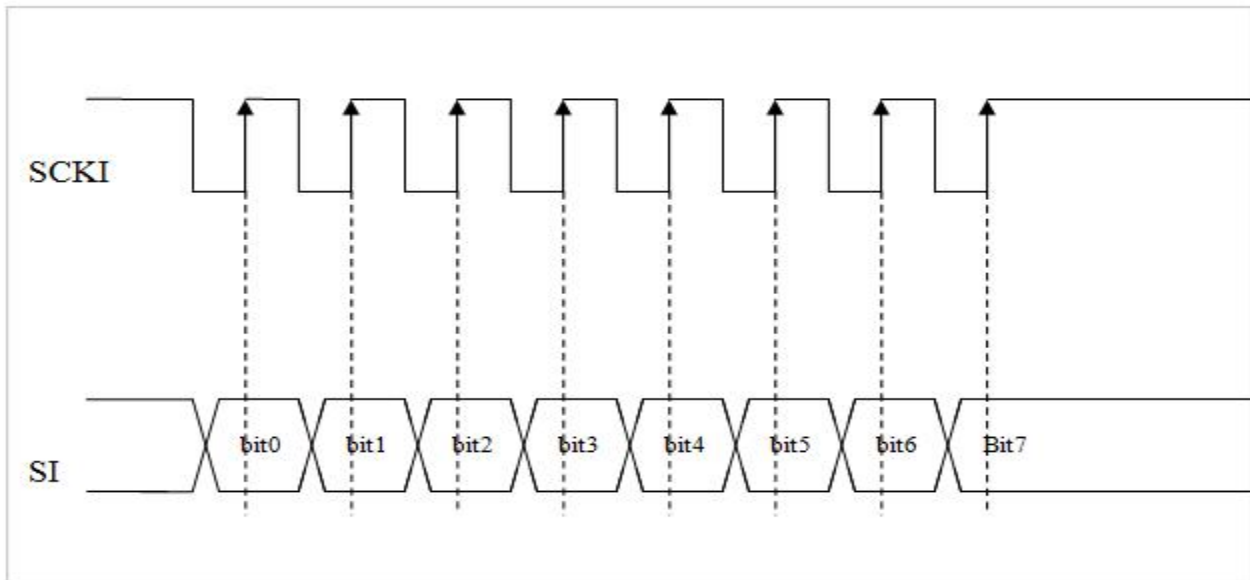


Figure 6.5 Receive data and capture timing with external clock

A receive operation is carried out as follows:

6. Set bit SIE to 1 in SIOR to select the SI pin function.
7. Clear bit SCN1 in SCR to 0, set bit CKS3 to 1 and set bit SNC0 to 0 or 1, designating 8-bit or 16-bit synchronous transfer mode.
8. Set the SCSR start flag (STF) to 1. SCIA starts operation and receives data at pin SI.
9. After data reception is complete, bit IRR in SSR is set to 1.
10. Read the received data from SDRL SDRU as follows:
 - 8-bit transfer mode: SDRL
 - 16-bit transfer mode: Upper byte in SDRU, lower byte in SDRL

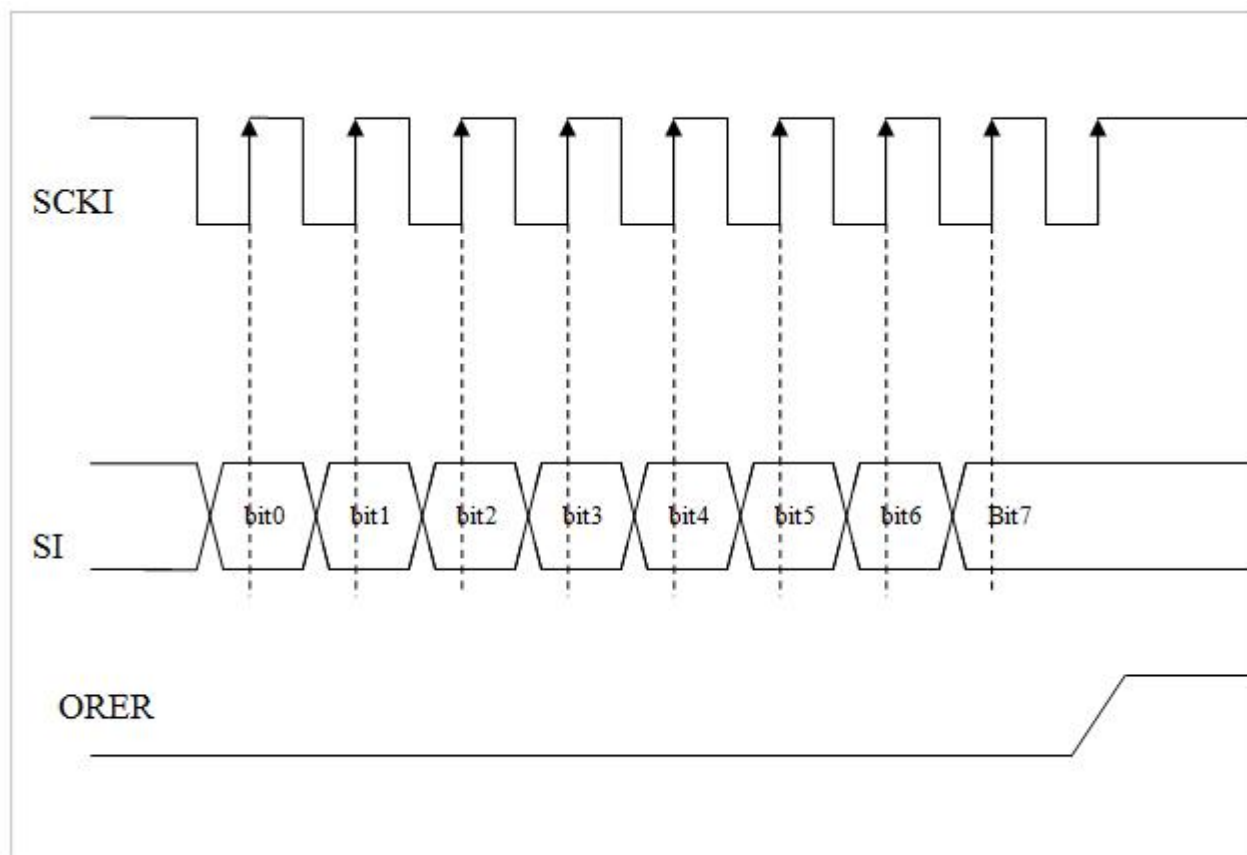


Figure 6.6 Overrun occurs in reception with external clock

After data reception is complete, an overrun occurs if the serial clock continues to be input; no data is received and the SCSR overrun flag (bit ORER) is set to 1.

6.3 Simultaneous operation (transmit/receive)

Actually, above mentioned 2 operations can be executed at the same time.

6.3.1 Internal clock

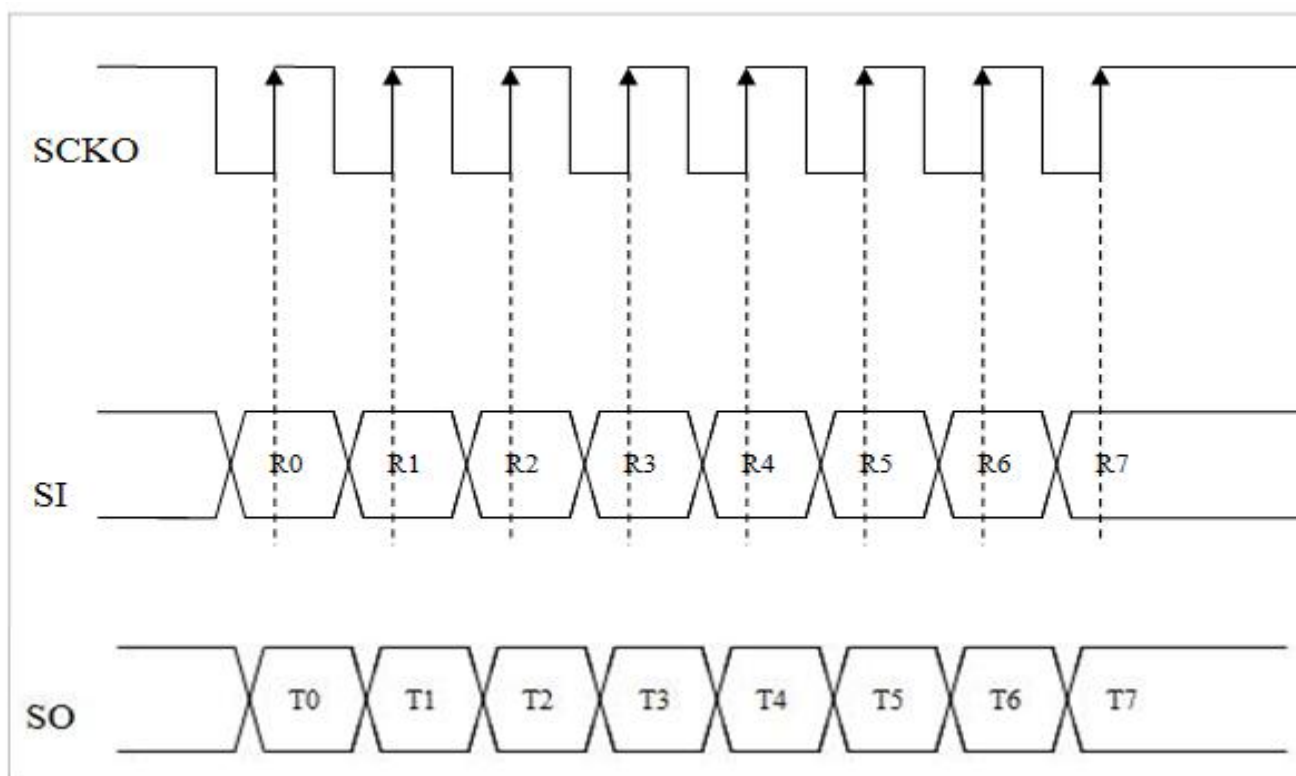


Figure 6.7. Simultaneous transfer timing with internal clock

1. Set bits SOE, SIE and SCKE to 1 in SIOR to select the SO, SI and SCK pin functions.
2. Clear bits SNC1 and CSK3 in SCR to 0, set bit SNC0 to 0 or 1, designating 8-bit or 16-bit synchronous transfer mode. Select the serial clock in bits CKS2 to CKS0.
3. Write transmit data in SDRL and SDRU as follows:
 8-bit transfer mode: SDRL
 16-bit transfer mode: Upper byte in SDRU, lower byte in SDRL
4. Set the SCSR start flag (STF) to 1. SCIA start operation. Transmit data is output at pin SO. Receive data is input at pin SI.
5. After data transmission and reception are complete bit IRR in SSR is set to 1.
6. Read the received data from SDRL and SDRU as follows:
 8-bit transfer mode: SDRL
 16-bit transfer mode: Upper byte in SDRU, lower byte in SDRL

A serial clock is output from pin SCKO in synchronization with the transmit data. After data transmission is complete, the serial clock is not output until the next time the flag is set to 1. During this time, pin SO continues to output the value of the last transmitted bit.

While transmission is stopped, the output value of pin SO can be change by rewriting bit SOL in SCSR.

6.3.2 External clock

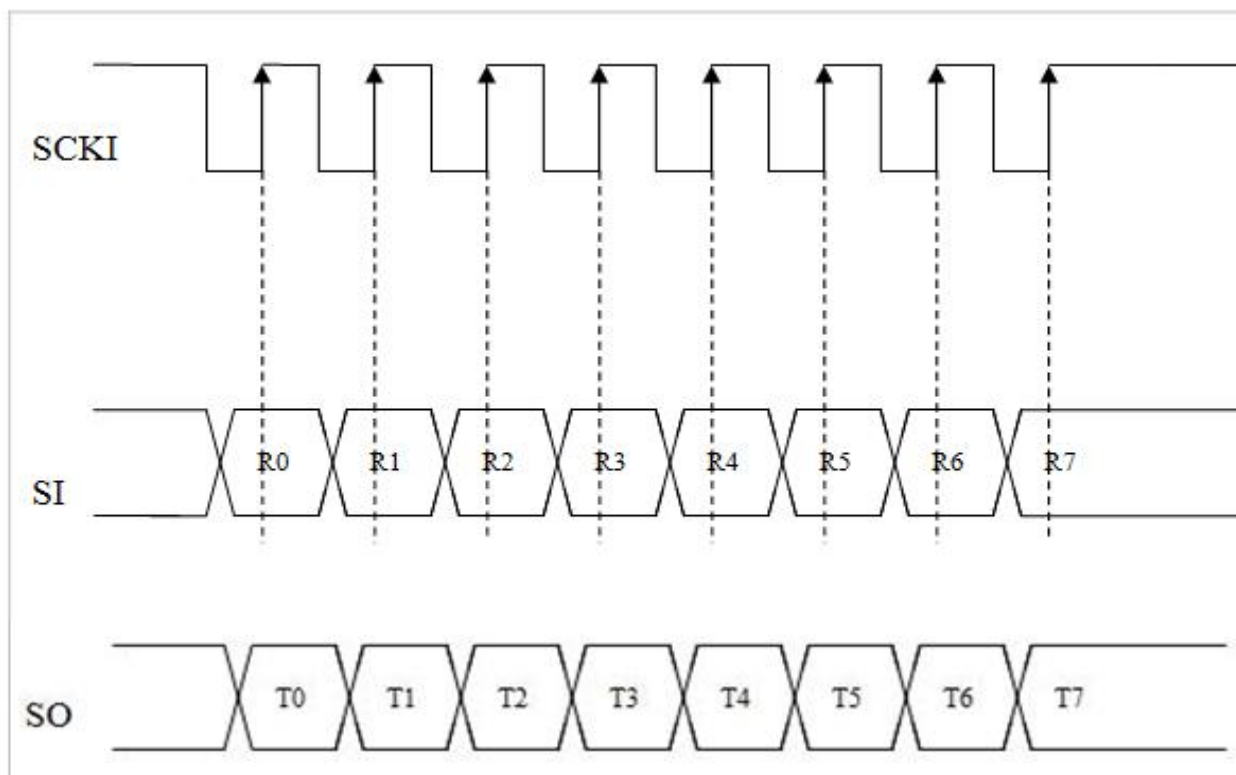


Figure 6.8. Simultaneous transfer timing with external clock

1. Set bits SOE, SIE to 1 in SIOR to select the SO, SI pin functions.
2. Clear bit SNC1 in SCR to 0, set bit CKS3 in SCR to 1, set bit SNC0 to 0 or 1, designating 8-bit or 16-bit synchronous transfer mode.
3. Write transmit data in SDRL and SDRU, as follows:
 8-bit transfer mode: SDRL
 16-bit transfer mode: Upper byte in SDRU, lower byte in SDRL
4. Set the SCSR start flag (STF) to 1. SCIA starts operation. Transmit data is output at pin SO. Receive data is input at pin SI.
5. After data transmission and reception are complete, bit IRR in SSR is set to 1.
6. Read the received data from SDRL and SDRU as follows:
 8-bit transfer mode: SDRL
 16-bit transfer mode: Upper byte in SDRU, lower byte in SDRL

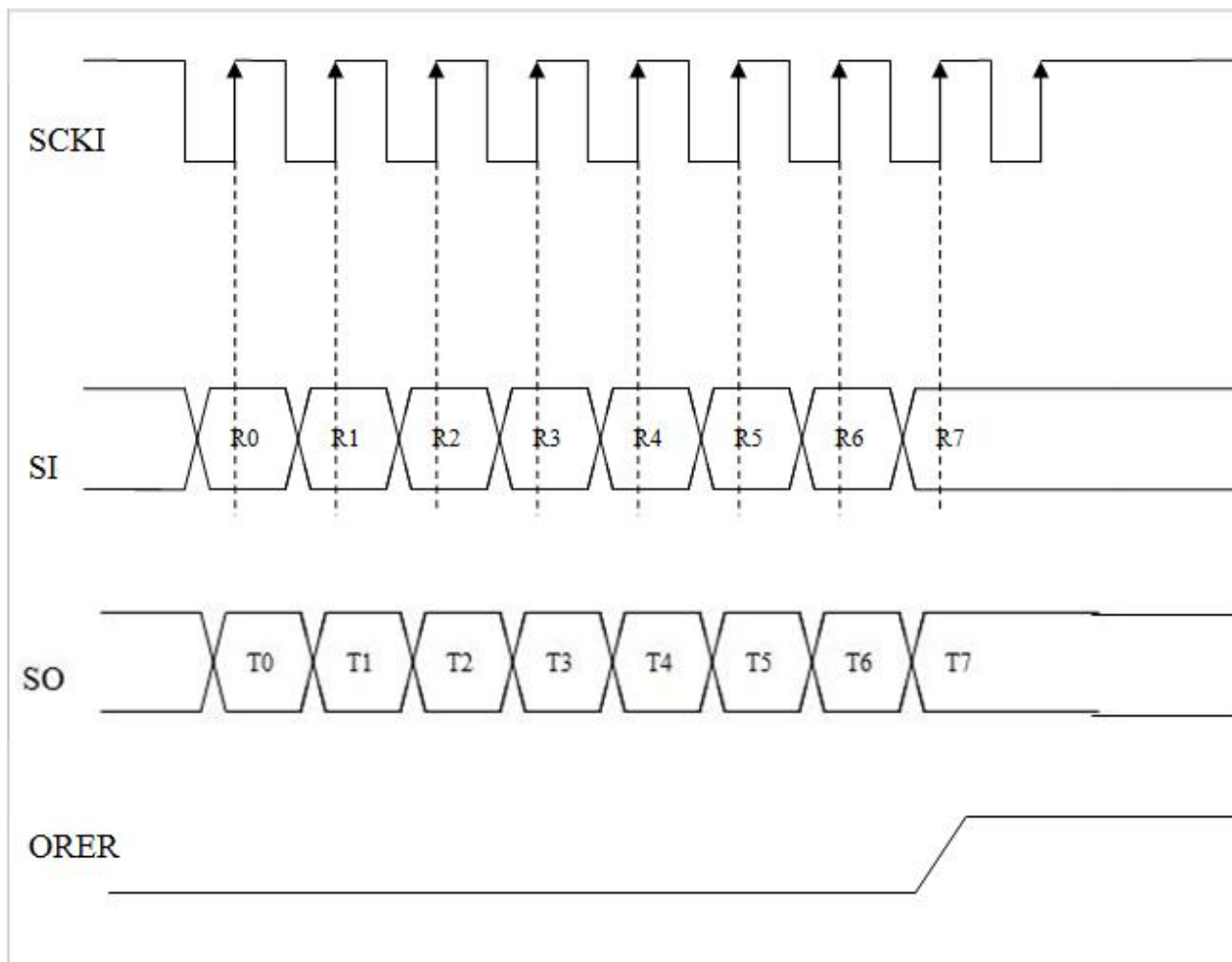


Figure 6.9 Overrun occurs in simultaneous transfer with external clock

Data is transmission and receive in synchronization with the serial clock input at pin SCKI. After data transmission and reception are complete, an overrun occurs if the serial clock continues to be input, no data is transmitted or received and the SCSR overrun error flag (bit ORER) is set to 1.

6.4 Continuous clock output

SCIA doesn't transfer any data in this operation. This operation is only for outputting clock continuously.

6.5 Interrupt request output timing

SCIA has an interrupt request flag (IRR) and can output the interrupt request (sc_txi) after completing transfer.

Bit IRR id SSR is set when SCIA finishes transferring. And if bit IEN of SIER is asserted, sc_txi is asserted.

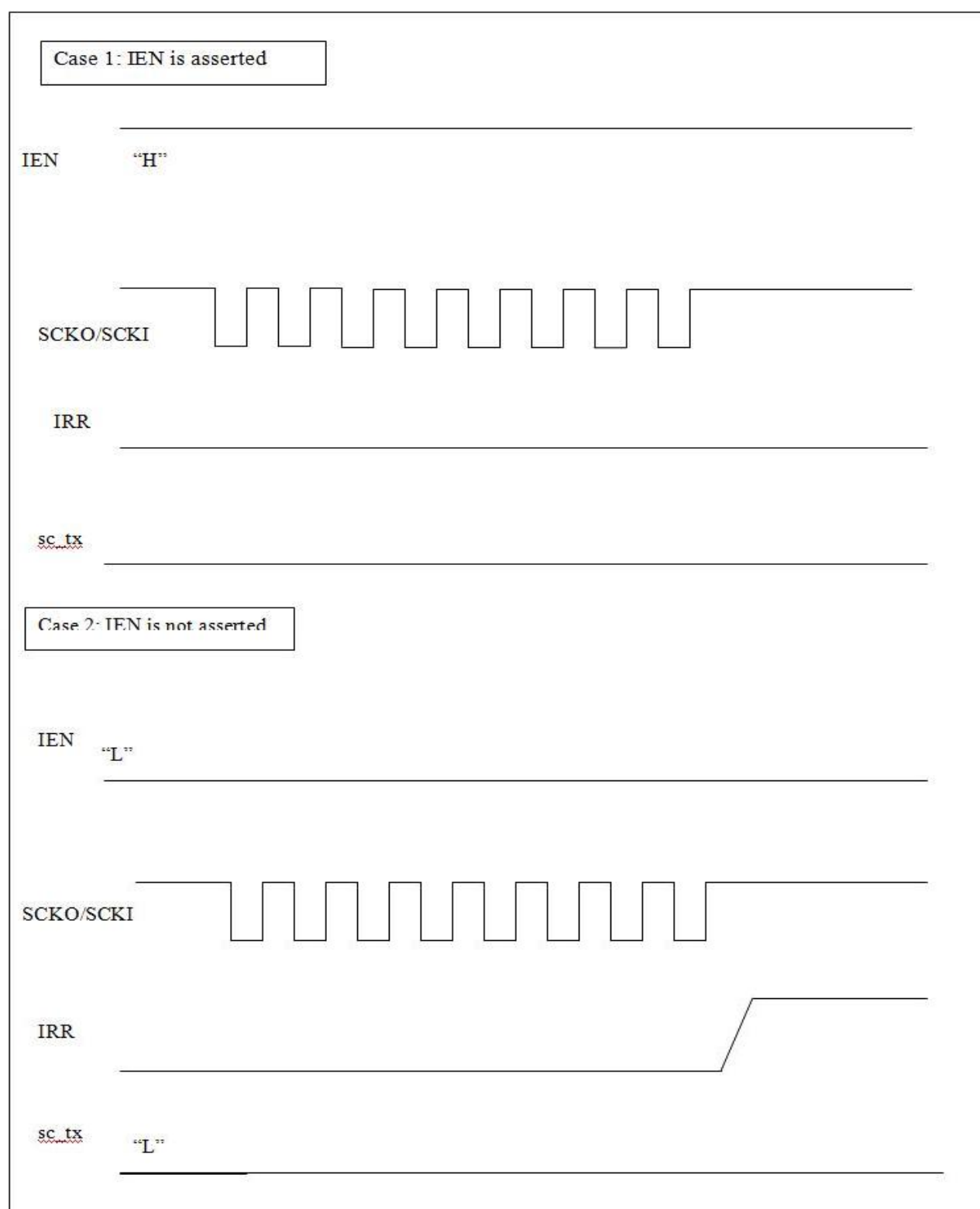


Figure 6.10. Interrupt request output timing

6.6 Stop operation

If CPU writes to SCR or SCSR while transferring, the transfer operation is stopped. Because the internal logic returns to initial state, user can-restart transferring after setting register.

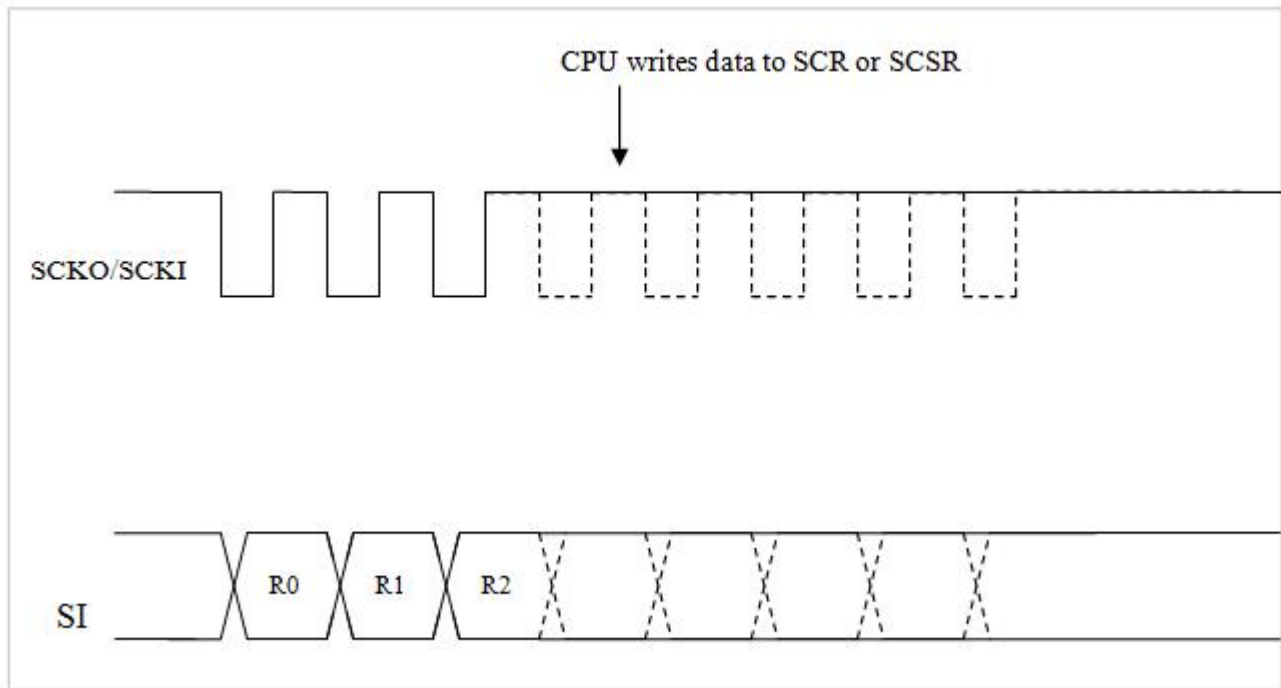


Figure 6.11. Stop operation timing

--End--